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Invited Review Paper

Present Status and Prospect of Si Wafers for Ultra Large Scale Integration

Hideki TSUYA

Si wafers have contributed to the rapid growth of the semiconductor industry as a basic material for ultra large scale integration (ULSI) through the research and development of new technologies and mass production in response to the various demands of device manufacturers. In this paper, first, the key issues of wafer quality improvement with respect to wafer fabrication technology, gettering and grown-in defects are reviewed. Various wafers currently in use such as annealed wafers, epitaxial wafers and 300 mm diameter wafer are discussed with respect to technology and cost effectiveness. Advanced Si-based wafers represented by silicon on insulator (SOI) and strained SiGe wafers are also described. After discussing the challenge to develop innovative Si wafer technologies which will lead to the future development of ULSI, the other important issues associated with Si wafers such as the re-examination of over-stringent specifications, cost reduction, economically reasonable pricing and the promotion of mutual understanding and cooperation between device makers and wafer makers for the continued development of both industries are emphasized.

Keywords: Si wafer, ULSI, SFQR, particle, gettering, grown-in defect, COP, annealed wafer, epitaxial wafer, 300 mm wafer, SOI, SIMOX, Bonding SOI, strained SiGe

1. Introduction

The International Technology Roadmap for Semiconductors (ITRS), which was released in 2001, states that miniaturization will proceed by a factor of 0.7 every three years until 2016.[1] However, the technological prospect is not necessarily clear. Beyond the 45nm node, it may be difficult to use optical lithography. Furthermore, in order to realize Moore's law, the introduction of new materials, for example, high-dielectric gate materials is inevitable. So to speak, we are now proceeding toward a new age governed by materials.

At the same time, the semiconductor industry is expanding onto the global stage and requires major investments, and thus collaboration and cooperation among companies on the worldwide scale as well as domestically are being accelerated. In addition, the foundry industry is growing and the worldwide share is drastically changing every year. It is clear that the semiconductor industry at the beginning of the 21st century is facing a major turning point in terms of business and technology.

Against this background, the silicon wafer industry, of which about 70% is occupied by Japanese-capital companies, has contributed to the growth of the semiconductor industry by providing the basic material for ULSI through the research and development of new technologies and mass-production techniques of Si wafers in response to the various demands of device manufactures.

Today, the quality requirements for Si wafers are divided into two categories. One includes universal qualities such as flatness and particle which are demanded by the ITRS roadmap. The other includes nonuniversal qualities such as gettering ability and shape/brightness of the back surface of a wafer, which strongly depend on the device processes employed. These qualities are closely correlated to the device fabrication tools used and the requirements differ among device manufactures.

On the other hand, the cost reduction of semiconductor devices is an absolute necessity, which requires both higher quality and cheaper wafers. In order to meet these requirements, cost reduction technologies in the mass production of wafers have been developed.

SOI wafers for low-voltage and low-power consumption devices are highly anticipated. According to the SOI roadmap, the thickness of the Si top layer will continue to become thinner, and 10–15 nm thickness and a uniformity of ±5% are requested. The strained SiGe/SOI heterostructure is a promising candidate for channel engineering to obtain a higher carrier mobility. The practical use of new Si-based materials is in the near future expected. In this paper, the present status of Si wafers for ULSI is reviewed and their future prospects are addressed.

2. Effect of Crystal Quality on Device Performance

After the establishment of dislocation-free Czochralski (CZ) Si crystal growth technology by Dash,[2] the greatest concerns in the early 1980s were oxygen impurities and the control of oxygen-induced bulk microdefects (BMDs). Intrinsic gettering (IG) using oxygen precipitates, of which the concept had already been proposed by Tan *et al.*[3] in 1977, was in practical use in the late 1980s.

A new type of grown-in defect, which was named the crystal originated particle (COP) by Ryuta *et al.*[4] in 1990, was found to

2-44-44 Fujigaoka, Aoba-ku, Yokohama 227-0043, Japan
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degrade device performance and yield due to the nearly same size as the design rule, and it has attracted much attention. Thereafter, the formation mechanism and the control/suppression of COP were extensively investigated.

Near-surface crystalline defects and metal contamination which cause device failure have been troublesome issues to the volume production engineers of device manufacturers. For example, defects-related oxygen precipitates inject minority carriers, resulting in the holding time failure of dynamic random access memory (DRAM).[5] Dislocation half-loops generated by film-edge-induced stress are one of the main causes of white spot defects of charge coupled device (CCD).[5] Furthermore, Fe and Cu impurities which nucleate at the interface of SiO_2-Si as metallic α-$FeSi_2$ and Cu-rich silicide, respectively, cause the breakdown of SiO_2 film.[6,7]

Gettering technologies are extremely effective for device yield enhancement, and their usefulness has been widely demonstrated in various devices. An example of the yield increase of DRAM using denuded zone IG (DZIG) wafers compared to natural IG (NIG) wafers is shown in Fig. 1.[5]

There have been many investigations concerning COP-induced device failures such as the degradation of isolation characteristics,[8,9] gate oxide integrity (GOI) failure,[10,11] the short fail of deep trench cell-based DRAM[12] and so on. If COPs exist in the isolation region, local oxidation of silicon (LOCOS) area with a residue of Si_3N_4 film is formed during the etching process, resulting in the isolation failure.[8] The thinning area of the field oxide film caused by COP increases the subthreshold leakage current markedly between the adjacent memory cells, resulting in the degradation of the isolation characteristics.[9]

In order to investigate the effect of COP on GOI failure, the I–V characteristics were measured for each metal oxide semiconductor (MOS) capacitor diode containing one COP and no COP of which the position were determined using a laser particle counter.[11] As shown in Fig. 2, the GOI yield more than 11 MV/cm for MOS diodes with one COP was 5 to 15%, and that for MOS without a COP was more than 95% for three kinds of crystals. The cross-sectional transmission electron microscopy (XTEM) observation of the V-grooved oxide layer showed the thinning of oxide on {111} which is related to the GOI failure due to the focusing of the electric field.[11]

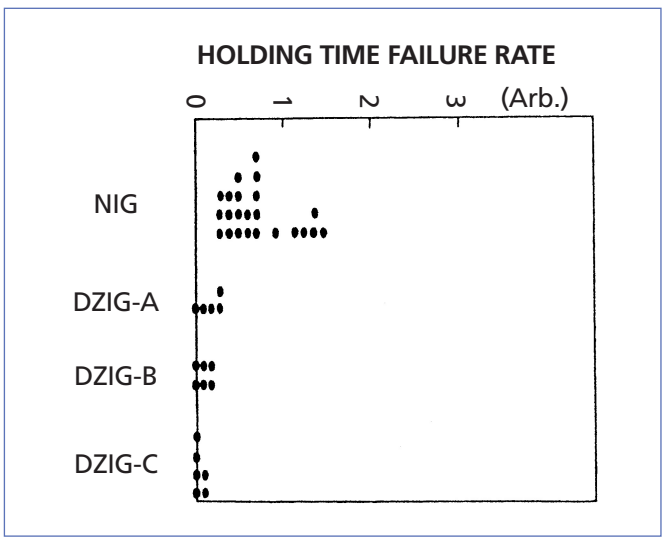

Fig.1. Holding time failure rate of DRAM for DZIG and NIG wafers.[5]

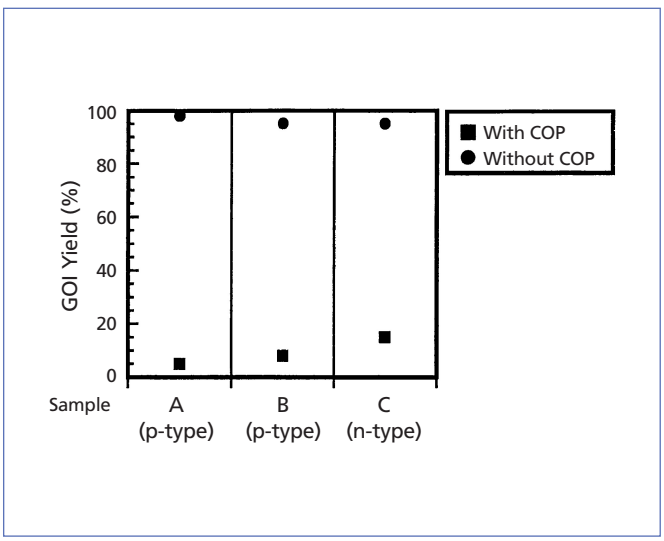

Fig.2. GOI yield for MOS capacitors of 25 nm oxide thickness and 1 mm^2 electrode area with COP (n=100) or without COP (n=50) on three kinds of crystal wafers.[11]

3. Key Issues for Wafer Quality Improvement

3.1 Wafer fabrication technologies

The requirement for wafer flatness and particle is becoming still more stringent with decreasing design rule. The ITRS requires that site flatness (SFQR) is comparable to or less than the design rule.

Silicon wafer fabrication technologies have not changed substantially over the past forty years. However, in order to improve flatness and reduce cost, new fabrication technologies have been introduced step by step. A low-damage surface grinding process was adopted to overcome the problem of free abrasive lapping damage. This process is an etchingless one and has the potential to be applied without the degradation of flatness induced by etching processes. Double-side polishing (DSP), where a wafer is unconstrained and is freely moving, realizes the highest polish quality and is inevitable to the manufacture of all 300mm wafers.[13)]

Newly adopted shallow trench isolation (STI) using SiO_2 deposited by chemical vapor deposition (CVD) instead of LOCOS is achieved by using chemical mechanical planarization (CMP). Silicon front surface topography variation, called nanotopography, which involves nanometer level waviness on a lateral range of a few millimeters up to centimeters, deteriorates the remaining oxide layer thickness uniformity after CMP, resulting in degraded isolation performance.[14)] DSP wafer is a solution for the problems associated with nanotopography.

The microroughness and reflectivity of the back surface of a wafer are important issues for device processes. For the lithography process, the microroughness of the back surface which meets the shape of stepper chuck is required. In the case of the dry etching process in which a wafer is chucked electrostatically, the microroughness of the back surface affects on thermal conductivity, resulting in incorrect temperature measurements. To date, acid etching has mainly been used. Recently, alkaline etching has become more favorable because it improves SFQR and nanotopography, but the microroughness is enhanced by the presence of facets.[15)] Minor process tuning may therefore be necessary.

3.2 Gettering

3.2.1 Gettering technologies and the current understanding of mechanisms

The gettering technologies, which eliminate unwanted heavy metal impurities from the device active region and capture them at gettering sites, have been widely used as a necessary key technology for the improvement of device yield and reliability. In particular, IG and polysilicon back sealing (PBS) gettering utilizing the grain boundary and defects of polysilicon deposited on the back surface of a wafer[16)] as well as gettering using a p/p^+ epitaxial wafer are currently employed on device mass-production lines.

Physical gettering mechanisms are classified into three types; relaxation-induced gettering, segregation-induced gettering and injection-induced gettering.[17)] IG occurs through the diffusion of supersaturated impurities from the device active region to the heterogenous nucleation gettering site due to the concentration gradient between the two sides. When the impurity concentrations for the two sides reach the solubility limit, gettering is achieved. The supersaturated condition is relaxed, and therefore this is called relaxation-induced gettering. The mechanism was confirmed on the basis of the low-temperature Fe-precipitation kinetics at silicon oxide precipitates.[18)]

PBS gettering, which was found to occur even under the unsaturated conditions of Cu and Fe, is understood as segregation-induced gettering[19)] due to the enhanced metal-solid solubility.[20)] The segregation of metal impurities proceeds at lower temperatures and at more gettering sites.

In the case of heavily boron doped epitaxial wafer, Fe impurities are strongly gettered by the Fe^+-B^- pair formation. The concentration of Fe^+ increases at lower temperatures and with the larger difference in Fermi energy between the epitaxial layer and the bulk induced by the difference in boron concentration between them. Therefore, this is called Fermi-level-induced gettering,[21)] and the physical mechanism is classified experimentally as segregation-induced gettering.[22,23)]

The p/p^+ epitaxial wafer is effective for Cu gettering,[24)] but the gettering efficiency is weaker than for Fe, because the dissociation energies for the Cu–B pair and for the Fe–B pair were reported to be 0.61eV[25)] and 1.40eV,[26)] respectively. Ni is not gettered by the p/p^+ wafer because of uncharged Ni^0 species,[24)] which requires BMD formation beforehand. A heavily boron doped wafer easily generates many BMDs.[27)]

Practically, various kinds of metal impurities are targeted. The key parameters such as solubility, diffusion coefficient and temperature must be considered. Figure 3 shows the dependences of the solubility of Ti, Fe and Cu on their diffusivity. From this figure, the process window of relaxation gettering is deduced for the target bulk contamination level of metals of 10^{10} atoms/cm^3.[28)]

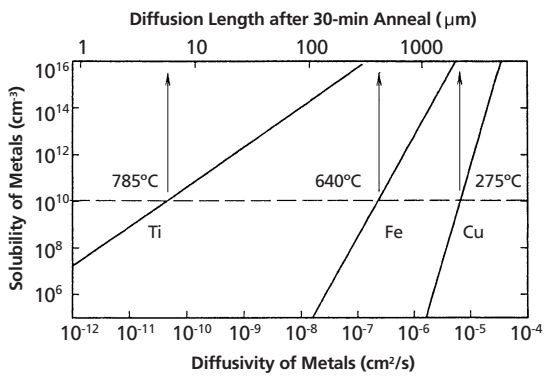

Fig.3. Dependences of the solubility of Ti, Fe and Cu on their diffusivity. The dashed horizontal line corresponds to the target bulk contamination level of metals of 10^{10} atoms/cm^3.[28)]

3.2.2 Advanced gettering technologies

The favorable gettering technologies have been selected from the point of view of device miniaturization and device processes. DSP wafers and rapid thermal processing (RTP) using low temperatures are necessary for advanced devices, and epitaxial wafers are extensively adopted. Therefore, IG and p/p$^+$ Fermi-level-induced gettering will survive.

It is difficult to expect that many oxygen precipitates are generated during low-temperature device processes due to the suppression of BMD growth. Figure 4 shows the gettering behaviors for initial Ni contamination in the high- and low-temperature processes.[29] Ni silicides are dissolved and gettering proceeds during the drive-in process through BMDs formed in the high-temperature process. The generation lifetime measured by MOS-Ct recovers to the same level of no Ni contamination, but in the low-temperature process, lifetime is degraded, and thus it is critically important that the gettering sites should be optimized in the early stages of the device process.

Recently, progress has been made with the simulation of gettering. It is possible to predict the oxygen precipitation behavior by introducing parameters such as process conditions, thermal history of a crystal and initial oxygen concentration into the Fokker–Plank equation.[30] Using the critical size and density of oxygen precipitates for IG occurrence, which are obtained from computer simulation and experimental data, IG effect is able to be predicted in the actual device processes. Figure 5 shows an example of the IG prediction for Ni in p/p$^-$ wafers with IG and without IG.[31] This prediction is also confirmed by generation lifetime measurement.

Many vacancy agglomerates are formed by quenching a silicon crystal from a high temperature in an Ar atmosphere.[32] Recently, by controlling the vacancy concentration profile at 1250°C for 30s in Ar using a RTP tool, a new type of silicon wafer with DZ and oxygen precipitates for IG, which is named the magic denuded zone (MDZ) wafer, was developed.[33] The soaking temperature, quenching conditions and ambient gas are important parameters.

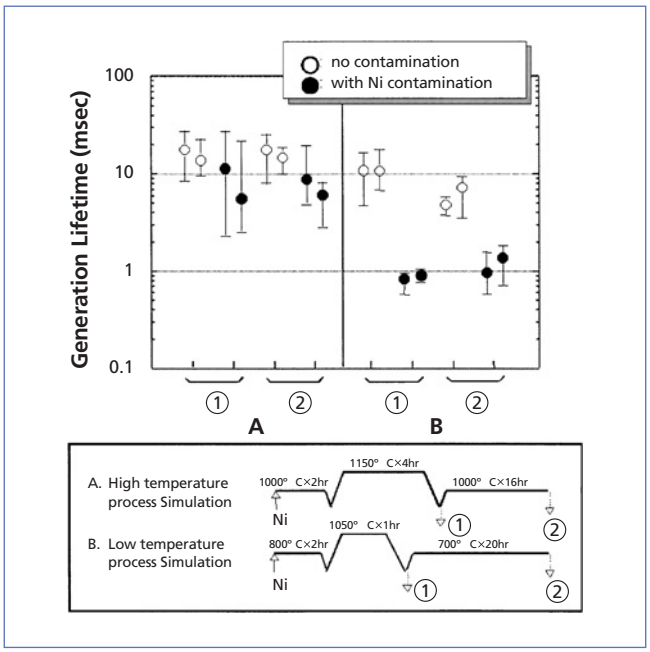

Fig.4. Gettering behaviors for initial Ni contamination (1×10^{12} atoms/cm^2) in the high-temperature process and in the low-temperature process.[29]

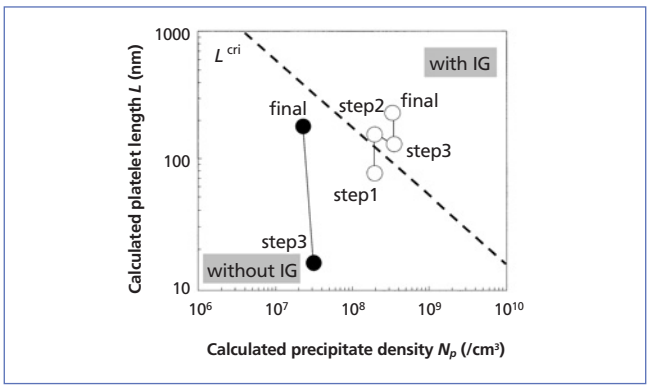

Fig.5. Example of IG prediction in p/p$^-$ wafer without IG (●) and p/p$^-$ wafer with IG at 900°C for 1h before epitaxial process (○). Process sequence is 800°C/4h (step 1) + 1000°C/2h (step 2) + 750°C/4h (step 3) + 1000°C/2h (final).[31]

3.3 Grown-in defects

3.3.1 Structures and features

The origin of COP is the singularities observed by a laser particle counter as small particles which are not dust on the wafer but pits delineated by repeated SC1 cleaning. It was suggested that such pits originate from defects in the melt-grown crystals.[4] Vacancy-related complexes were presumed from the existence of pits. Park *et al*.[34] observed voids of 0.25 to 0.50μm in diameter at the Si/SiO_2 interface of the B-mode type oxide breakdown classified by Yamabe *et al*.[35] The oxide defects were characterized to be octahedron structures full of vacancies by Itsumi *et al*.[36] using XTEM and energy-dispersive X-ray spectroscopy (EDX). Voids on a wafer surface are recognized as pits.

A number of investigations were performed on the wafers after the cleaning processes and heat treatment processes. Kato *et al*. observed for the first time the grown-

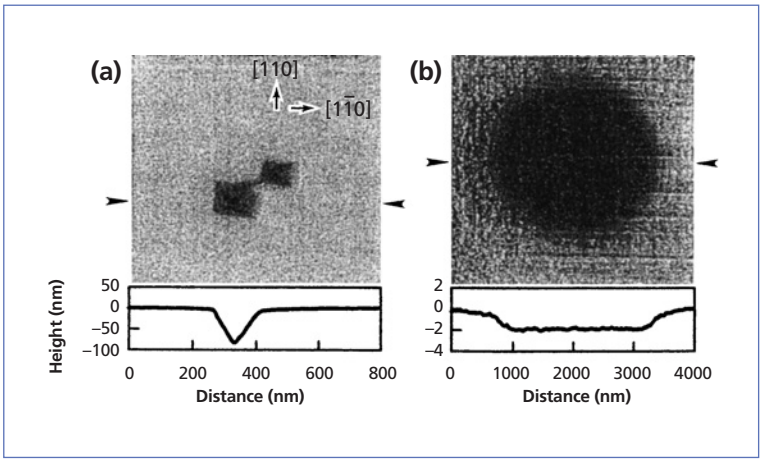

Fig.6. AFM images and cross-sectional profiles of COPs on the Si (001) surface after H_2 annealing. (a) as-received and (b) at 1100°C for 10min.[38]

in defects of as-grown crystals by TEM. The basic structure was to be found a composite of two or three incomplete octahedral voids, of which the walls are surrounded by several nanometer thick SiO_X.[37]

The shape of COP changes with heat treatment, and it finally disappears. Figure 6 shows typical atomic force microscopy (AFM) images and cross-sectional profiles of the (001) wafers, (a) as-received and (b) after heat treatment at 1100°C for 10min in H_2.[38] The COPs had disappeared completely after the annealing at 1100°C for 20min. Silicon atomic step etching caused by silicon atom evaporation in H_2 and surface reconstruction as well as silicon atom migration from the step edge to the bottom of the COP at high temperatures are the main causes for the change of COP shape.

3.3.2 Formation mechanism

With respect to the behavior of grown-in defects, it is important to understand the incorporation and diffusion of intrinsic point defects such as vacancies and self-interstitials. Voronkov proposed an excellent theory in which the type and concentration of dominant point defects after crystal growth depend on the ratio V/G, where V is the growth rate and G is the longitudinal temperature gradient near the crystallization temperature for floating zone (FZ) crystal.[39] His theory, based on the recombination and diffusion of point defects, predicts that vacancies are dominant if $V/G>\xi$ and self-interstitials are dominant if $V/G<\xi$, where ξ is a certain constant, and it also explains many experimental results for CZ crystals well.

In order to clarify the formation mechanism of grown-in defects in CZ crystals, two crystals were grown under extremely different growth conditions.[40] One was quenched during growth and the other was halted after growth. It was found that the size of the grown-in defects formed in the narrow temperature range of the halted crystal was much larger that of the quenched ones as shown in Fig. 7. This means that grown-in defects nucleate and grow in the narrow temperature range of about 30°C below 1100°C due to a rapid agglomeration of vacancies. It was also found that the growth of the oxide film in the voids is a rate-limited process limited by the diffusion of oxygen atoms. The formation process of the grown-in defects consists of two main steps, being the rapid void growth and the growth of oxide film on the inner wall as shown in Fig. 8.

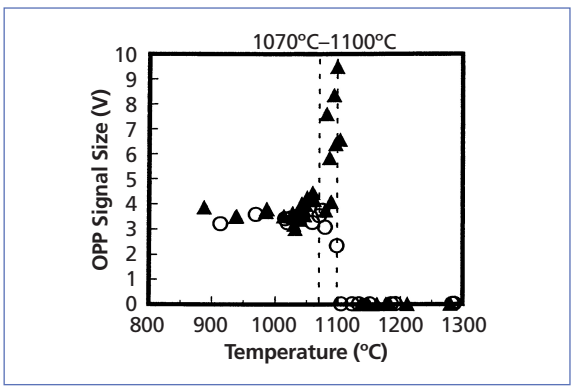

Fig.7. Distribution of optical precipitate profiler (OPP) signal size as a function of the crystal temperature just before quenching converted from the crystal axial position. ○ quenched, ▲ halted crystal.[40]

3.3.3 Control and suppression

Stacking faults with a ringlike distribution after thermal oxidation (R-OSF) are observed in some commercial wafers. The appearance of R-OSF depends on the crystal diameter and growth rate. For example, R-OSFs are not observed for growth rates less than 0.5mm/min or more than 1.0mm/min for 125mm crystals.[41] A distinct difference between the grown-in defect distributions inside and outside the R-OSF region with changing the growth rate was found using Secco-etching and light scattering tomography (LST).[42]

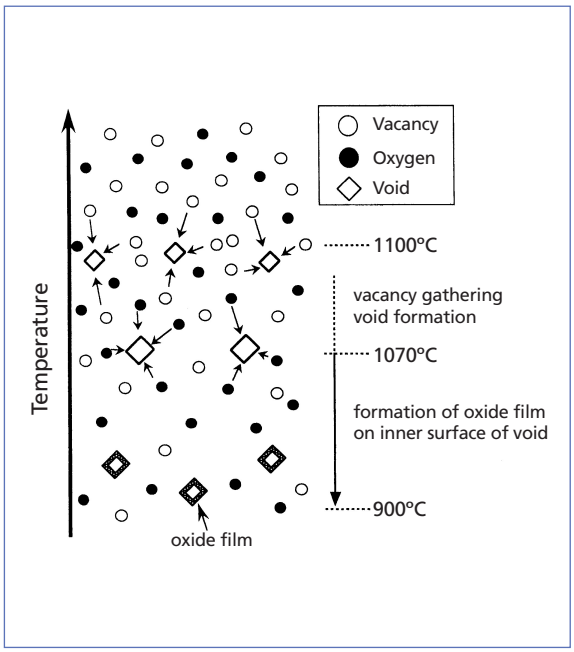

Fig.8. Schematic illustration of the grown-in defect formation.[40]

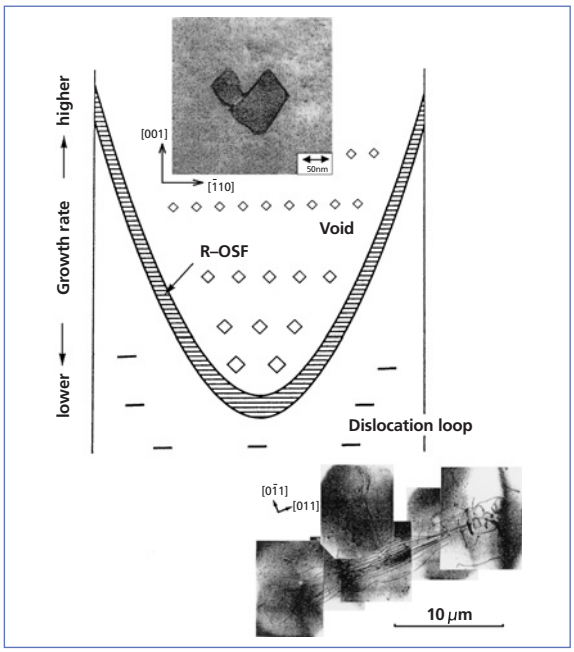

Fig.9. Schematic longitudinal cross-section distribution of grown-in defects versus growth rate including TEM image of void[37] and large dislocation loops.[42]

Considering Voronkov's theory and the previous findings for FZ silicon crystals,[43] it is widely accepted that the vacancy-related defects distribute inside the R-OSFs and the self-interstitial-related defects distribute outside the R-OSFs. Figure 9 shows schematically the longitudinal cross-sectional distribution of grown-in defects versus the growth rate, including TEM images of the voids[37] and large dislocation loops.[42]

In a conventional CZ furnace, G increases along the crystal radial direction due to the large heat radiation, and thus V/G decreases towards the crystal surface even for a constant V, resulting in dominant self-interstitials towards the outer region of a crystal.

For the suppression of grown-in defects, it is important to design the hot zone with a more radially uniform V/G and to control the growth parameters. By controlling the axial and radial V/G within certain critical values during crystal growth, "pure silicon wafer", which are none of agglomerate defects such as COPs and large dislocation loops due to the intrinsic point defects much less than the critical concentrations, have been developed.[44] Pure silicon wafers of 200mm diameter which are COP-free and large dislocation-free from top to bottom are now being in mass produced.[45]

Several critical values of V/G obtained experimentally and theoretically have been reported.[46–48] The reason for the scattered values may be the uncertainty of the observed values and of the constant values of point defects used in the calculation. In addition, the V/G value is shifted by the presence of impurities such as oxygen, carbon and nitrogen.[49,50]

Nitrogen doping enhances oxygen precipitate-induced defects,[51] which were found to be stable even after heat treatment at 1100°C.[52] It was also found that nitrogen doping affects the formation of grown-in defects, and the tolerance of the V/G value for the grown-in defects-free region was expanded particularly for the doping of more than 1×10^{14} atoms/cm^3.[50] This is explained by the reaction of nitrogen with point defects which serves to reduce the point defect concentration. Nitrogen doped wafers are favorable for the epitaxial wafer substrate.

4. Various Wafers Currently in Use

Here, current Si wafers, aside from the pure silicon and MDZ wafers are discussed.

4.1 Annealed wafers

The DZIG wafer and the H_2 annealed wafer[53] (called the Hi or HAI wafer) which were in practical use in the 1980s are kinds of annealed wafers for the enhancement of gettering ability and the defect-free near subsurface. In the late 1990s and the early 2000s, high-temperature annealed wafers for the suppression of COP were investigated and nitrogen doped wafers annealed in Ar were developed.

It is important in practice to expand the possible range of initial oxygen content and to homogenize the oxygen precipitation independent of thermal history.[54] A multistep heat treatment for IG (MIG, hereafter) after the high-temperature annealing for DZ for-

mation enhances the IG ability and homogenizes the oxygen precipitation.[55] Figure 10 shows the oxygen content of wafers from top to bottom of a crystal after each annealing process: (a) for two-step annealing and (b) for MIG (520°C+620°C+720°C, for each 16h) annealing.[5] The homogenization of oxygen precipitation is achieved after MIG annealing. In the case of a two-step annealing, the interstitial oxygens which precipitate incompletely after the first heat treatment proceed to precipitate during the second heat treatment, whereas almost all of the interstitial oxygens precipitate completely after the MIG annealing. After the final annealing at 1140°C, oxygen precipitates are partially redissolved and the interstitial oxygen content is close to the solubility limit.[56] A multistep heat treatment MIG is a prototype of DZIG wafer fabrication. To achieve cost reduction, MIG was replaced by a ramping annealing from a low temperature.

Furthermore, the Hi wafer was reported to eliminate COP perfectly even in the region deeper than 500nm by hydrogen annealing at 1200°C.[57] Argon annealing is also effective in the elimination of COP. The high-temperature annealings at 1200°C and 1300°C with a ramping rate of 1°C/min achieved the COP-free zones of 20μm and 100μm depth, respectively.[58] A shrinkage model of grown-in defects consisting of the dissolution of the oxide on the inner walls of defects and the subsequent injection of self-interstitials at a thermal equilibrium concentration was proposed.[58]

It was also found that the annealings in H_2 and Ar at 1200°C for 1h easily annihilate the COP of nitrogen doped wafers and a high density of BMDs still exist.[59] In this case the heating and cooling rates were 6 and 3°C/min, respectively. The annihilation was more effective to the initial smaller size of COP and at a lower oxygen content. The combination of rapid growth (1.8mm/min) and nitrogen doping was the optimum for achieving smaller voids and deeper void-free zone of 10μm.[59] The mechanism of BMD formation and void annihilation is explained by the model in which the morphology of voids changes from octahedral to plate shape triclinic, which nucleates oxygen precipitation for nitrogen concentrations above 4.6×10^{14} atoms/cm^3.[60] Under argon annealing, voids are annihilated and a high density of oxygen precipitates is generated stably.

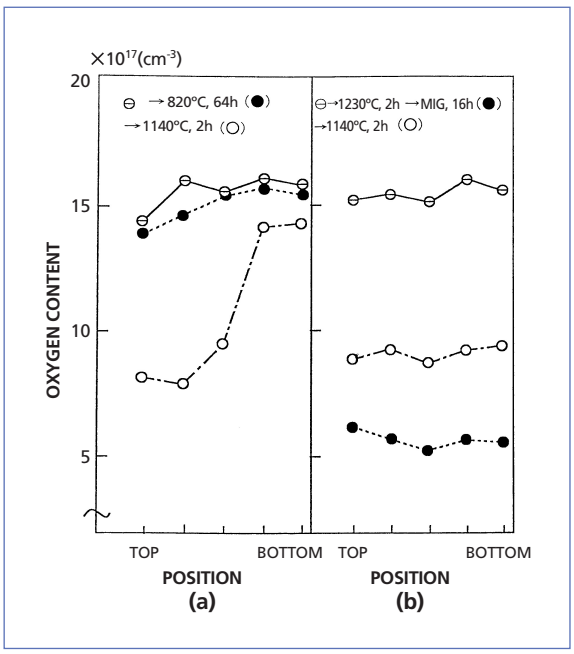

Fig.10. Oxygen content of wafers obtained from top to bottom of a crystal after each annealing process; (a) ⊖ as-grown; ● 820°C/64h; ○ 820°C/64h + 1140°C/2h, (b) ⊖ as-grown; ● 1230°C/2h + MIG; ○ 1230°C + MIG + 1140°C/2h.[5]

4.2 Epitaxial Wafers

Si epitaxy has a long history. Epitaxial growth technology has advanced with the progress of bipolar devices. Epitaxitial wafers with a thin epitaxial layer grown under low pressure have contributed to the realization of high-performance and high-speed bipolar devices. On the other hand, p/p$^+$ epitaxial wafers have been widely used in complementary MOS (CMOS) logic devices because of the effectiveness of the latch-up suppression[61] and of the noise reduction of analog and digital circuits[62] and also of the gettering of Fe. Epitaxial wafers have been used in memory devices such as 64MDRAM and flash memory and the production output has increased since 1997.

4.2.1 Features of epitaxial wafers

Epitaxial wafers have certain features which are different from that of bulk wafers. High-quality DZ is essentially formed because there is no fabrication surface damage and no oxygen precipitate-induced microdefects due to the extremely low oxygen content and the small number of precipitate nuclei. Furthermore, in many cases the COP disappears during epitaxial growth processes on the substrate with COP.

However, it is undeniable that some unique defects such as mounds and epitaxial stacking faults are generated during epitaxial growth.[63] These defects are usually evaluated using a light scattering system, and thus are called light point defects (LPD). Mounds are generated due to the foreign materials detached from the quartz chamber of the epitaxial reactor, and increase in number with decreasing growth temperature. Defects larger than 20μm diameter are called large area defects (LADs). Stacking faults are generated from the particles at the interface between the epitaxial layer and substrate. The relation between the substrate particles and the epitaxial defect morphology was investigated in detail.[64] The epitaxial defect morphology was found to change depending on the epitaxial layer thickness and particle size. The suppression of size and density of epitaxial defects is urgently demanded with the continuing de-

crease of the design rule, and continuous effort toward the improvement of production technology is required.

4.2.2 p/p$^+$ wafer

The back side of the p/p$^+$ wafer is covered with CVD-SiO_2 film in order to prevent boron autodoping from the substrate. The deposition of film is the cause of increase in cost and contamination. In the case of 300 mm wafers fabricated using the DSP process, the CVD process is not adopted. The epitaxial layer is usually grown using a horizontal single reactor at around 1100°C. The epitaxial growth at lower temperatures is promising for the prevention of boron autodoping.

Recently, a single epitaxial reactor of which the susceptor is rotated at the very high speed of 500–2000 rpm was developed.[65] It was reported that epitaxial layers grown at low temperatures of 900–1000°C and under 2–100 Torr, with a growth rate of 3–4 μm/min, were mound-free and uniform in thickness. This may be because the reaction efficiency of gas is increased and particles are blown off by the high-speed rotation of the susceptor.

The improvement of the susceptor and the epitaxial process is effective in the prevention of boron autodoping. The plurality of holes on the susceptor allows the boron atoms out-diffused from the back surface during epitaxial growth to be carried away in an inert gas stream from the front surface and into the exhaust such that the autodoping of the front surface is minimized.[66] The resistivity of the epitaxial layer without a CVD-SiO_2 film was uniform and comparable to one with a CVD-SiO_2 film.

4.2.3 Epitaxial wafer grown on nitrogen doped substrate

A COP-free epitaxial layer is grown in H_2 at above 1100°C, but under this condition the BMD density of the substrate decreases, resulting in the degradation of the gettering ability. Both freedom from COP and an effictive BMD density are necessary.

A nitrogen doped substrate is useful for epitaxial wafer because of the stability of the BMD density obtained after epitaxial growth. However, some defects happen to be generated in the epitaxial layer. Nakai *et al*. posited that epitaxial layer defects such as stacking faults and dislocations are generated due to void morphology changes and grown-in oxygen precipitates in nitrogen doped substrates with higher nitrogen concentration and lower *V/G*.[67] They have proposed that the optimization of nitrogen concentration and *V/G* value, and also carbon co-doping are effective for the prevention of epitaxial layer defects growth.[67]

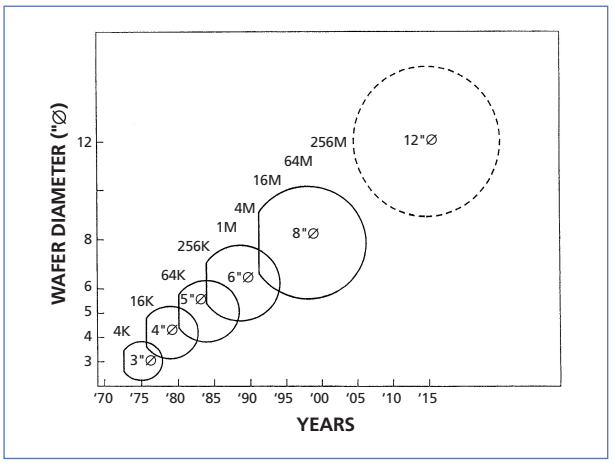

Fig.11. Trends in Si wafer diameter and packing density of DRAM.[69]

4 2.4 Cost reduction of epitaxial wafer

The cost reduction of epitaxial wafer is very important and four points are considered.[63] The cost of substrates has to be reduced. Substrates grown with high growth rate should be widely used and the severe limitation of the oxygen and boron concentration ranges should be relaxed. In the wafer fabrication process, is it necessary to use the same recipe as polished wafers? For example, Yamamoto reported that GOI failure caused by the wafer fabrication process is improved by using epitaxial wafer.[68] A simpler fabrication process may be adopted. A epitaxial reactor with high performance such as high productivity and low running cost is urgently demanded. As for the epitaxial growth process, the reduction of the epitaxial growth cycle time, wafer etch reduction and the saving of monitor wafers are key issues.

4.3 300mm (12 inch) wafer

As shown in Fig. 11, the diameter of silicon wafers increases by 1 inch every four years.[69] By extrapolating this trend, the mass-production age of 12 inch wafers is expected to be after 2005. (The mass-production age is tentatively defined as the year when the percentage of the production sheets of the target wafer occupies the 10% of all wafers from 4 inch to 12 inch). At present, the production of 12 inch wafers is increasing steadily. At the end of 2003, the production of 12 inch wafers in worldwide was estimated to be 3.4% of all wafers produced.

The wafer fabrication process technology for the 300 mm wafer is basically similar to that of the 200 mm wafer, but with the adoption of the DSP process, a superior flatness is achieved. The specification of SFQR and particle of polished 300 mm wafer for the 130 nm rule is already fulfilled.[70] The concept for the epitaxial reactor for 300 mm wafers is the same as that for 200 mm wafers, so there is no technical difficulties.

The issue causing the most concern is the crystal growth technology for heavy 300 mm crystals. In order to obtain the same yield as that for 200 mm crystals, the establishment of a growth technology for over 300 Kg weight crystals is necessary.[71] Here, the yield means the ratio of product weight to charge weight.

In addition, a quartz crucible with a large diameter of around 40 inches has to be developed for the pulling of long and heavy crystals.

It is impossible to support stably the heavy crystals of 300–400 Kg weight by the Dash necking method[2] using a necking part of 3–4 mm in diameter. The supporting method using the larger knob formed after necking[72] is currently in practical use. Recently, dislocation-free 150 mm crystals were grown using a seed of 7×7 mm^2 in size without Dash necking.[73] The seed doped with a boron concentration of 1×10^{18} atoms/cm^3 was used to prevent thermal shock. Furthermore, by co-doping Ge of 8×10^{19} atoms/cm^3 and B of 2×10^{19} atoms/cm^3, the misfit dislocation was suppressed and dislocation-free crystals were grown using a seed 15×15 mm^2 in size.[74] The application to a 300 mm crystal is expected.

The melt flow becomes more complex with increasing diameter due to various factors such as the large heat radiation from the melt surface and the increase of temperature at the crucible wall. Turbulent convection of a large silicon melt up to 300 mm diameter is discussed experimentally from the fluid dynamics.[75] The development of a numerical model combined with global heat transfer is expected,[76] and more precise values of thermophysical properties are urgently demanded.

Considering the crystal growth technology, the growth rate must be slower due to the concave shape of the solid-melt interface. The consumption of the quartz crucible increases, resulting in the increasing incorporation of oxygen. In addition, due to the another factor of thermal history different from 200 mm crystal, the oxygen precipitation/retardation/recovery phenomenon is different from 200 mm.[77] The stabilization of the heat flow is critically important, for example, using the magnetic Czochralski (MCZ) method developed by Hoshi *et al*.[78] A uniform oxygen concentration with a radial gradient of 5% or less has been reported using a cusp-type MCZ, which is also beneficial to the minimization of the emission of SiO_2 particles from the crucible wall.[79]

Another issue is the slip generation in a vertical furnace at high temperatures due to the large gravitation-induced bending stress and thermal stress. These issues have to be resolved while maintaining the level of productivity. The use of three point support[80] and a ring-like jig[81] in a vertical batch furnace can lead to the slip reduction. Recently, it was reported that nitrogen doped wafers pulled at high speed are resistive to slip generation at 1200°C when supported using ring-like SiC holders covered by CVD coating.[82] The suppression of the slip propagation is explained as being due to a high density of nanometer-sized nitrogen-induced precipitates.

5. Advanced Si-Based Wafers

5.1 SOI

5.1.1 Various SOI wafers

Various kinds of SOI structures have been developed. However, two SOI wafers; separation by implanted oxygen (SIMOX) and bonding SOI wafer are in use at present. Although many new materials and processes have been developed over a long period, a genuine technology which overcomes the competitive ones can survive. These SOI wafers as leading substrates are promising for the coming high-speed, low-voltage and low-power consumption devices.

In 1978, Izumi *et al*. developed a new isolation structure using a high-dose oxygen ion implantation of 2×10^{18}/cm^2 and high temperature annealing at 1150°C, and realized a high-performance 19-stage CMOS ring oscillator fabricated in the SOI on the buried oxide (BOX) layer.[83] This is called SIMOX and it is one of the fundamental structures of SOI.

In order to reduce a high density of dislocations and fabrication cost of SIMOX wafer, various investigations have been carried out. A BOX layer formed with a dose 1/5 lower than that used previously was actively oxidized at 1350°C, resulting in internal thermal oxide (ITOX) formation on the BOX layer.[84] Using this method, the thickness of the BOX layer was increased and the morphology of the interface between the top Si and the BOX layer was greatly improved. Another approach which uses lower energy oxygen implantation at 65 keV with the dose reduction of 2×10^{17}/cm^2 achieved SIMOX wafers of higher quality.[85] SIMOX technology is suitable for ULSI, because the top Si layer with great thinness and high uniformity in thickness can be achieved simply by controlling the acceleration energy of the ion implantation.

A bonding SOI is fabricated by sticking two wafers of which one is thermally oxidized and by annealing at around 1100°C for 2h in O_2, followed by grinding and polishing the active SOI. The prototype of the bonding SOI was invented by Nakamura in 1961.[86] Bonding SOI with thick top Si layer is widely used in high-power devices.

Since the new fabrication methods using epitaxial growth and ion implantation processes have been introduced, bonding SOI wafers have received much attention for ULSI. The technological features of the epitaxial layer transfer (ELTRAN) wafer[87] are epitaxial growth on porous silicon, splitting by water jet, etching with extremely high selectivity and hydrogen annealing to achieve smoothness of the epitaxial layer. The controllability and uniformity of the top Si layer are excellent because of the use of epitaxial growth. The achievement of an ultrathin top Si layer of 55±2.1 nm by controlling the epitaxial growth has been reported for the 200 mm wafer.[88]

Another type of bonding SOI wafer fabricated using a smart-cut process[89] features hydrogen ion implantation for the delaminating layer formation underneath the SiO_2 layer and annealing at 600°C for splitting. A high-quality top Si layer is obtained by touch polishing. Cost reduction is expected because of the re-use of wafers, but the uniformity of the delaminating layer may be uncertain.

The issue of SOI wafers is the development of fabrication technology for the cost reduction of 300 mm. It is reported that the uniform thickness of 147±1.6 nm, which corresponds to ±1.1%, of the top Si layer is achieved for the ELTRAN 300 mm wafer.[90] As for bonding SOI using the smart-cut process, the uniformity of 200±20Å of the top Si layer

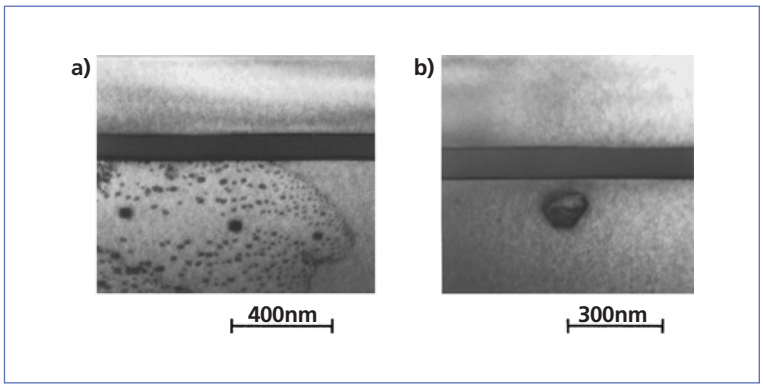

Fig.12. XTEM images of (a) Cu:Si precipitate colonies and (b) $NiSi_2$ precipitate formed beneath the BOX layer of SIMOX wafers. Surface metal contaminations of Cu and Ni are 2×10^{15} atoms/cm^2 and 5×10^{12} atoms/cm^2, respectively. Diffusion temperature and time are 950°C and 30min, respectively.[92]

in terms of wafer-to-wafer and on-wafer for 300mm is reported.[91] The uniformity of the SIMOX wafer is superior in principle.

5.1.2 Gettering in SOI wafers

The gettering phenomenon in SOI wafers is a critically important issue. The SiO_2 layer underneath the top Si layer prevents the diffusion of almost all metal impurities into the bulk substrate, resulting in a condensation of metals within the top Si layer. In the case of Cu and Ni, it was found that a BOX layer does not prevent diffusion from the top Si layer into the bulk substrate in the temperature range from 600°C to 900°C. These metals are gettered due to the heterogenous impurity precipitation at stacking fault tetrahedral formed during SIMOX implantation processes as metal silicides as shown in Fig. 12.[92] On the other hand, the BOX layer itself is an effective barrier against Fe diffusion, and thus the extended defects associated with oxygen implantation are less effective for Fe compared to Cu and Ni.[93] It has been noted that PBS gettering is efficient for Fe at temperatures higher than 1150°C during wafer processing,[94] due to the poor quality of the BOX layer. However, during device processing, PBS gettering may be surely inefficient because perfect BOX layer is already formed.

Lateral gettering by introducing crystalline defects in the vicinity of the device region is effective for achieving the metal capture. Many investigations have been carried out.[95–97] For example, significant improvement of the GOI was achieved by employing the Si implanted gettering sinks at the source and drain regions prior to gate oxide growth.[95] Both implantation-induced dislocation loops and P diffusion for lateral gettering sinks were reported to be effective for GOI improvement for all SOI types.[96]

5.1.3 SOI/bulk patterned structures and SON

The patterned structure of the hybrid SOI and bulk for achieving good performances of both DRAM and logic devices is interesting. Patterned SOI wafers were fabricated by masking out the oxygen implantation from the bulk regions during SIMOX processing.[98] DRAM and logic devices were fabricated on the bulk and SOI areas, respectively. The high-performance SOI-based logic-embedded DRAM was successfully demonstrated. Another approach is the combination of selective etching with a nitride mask and selective epitaxial growth on a bonding SOI wafer.[99] DRAM embedded in SOI devices attained equal data retention characteristics to those for the bulk, while maintaining the superior SOI performance.

Traditional SOI is fabricated on a BOX layer having the dielectric constant of 3.9. However, the ideal structure is a buried air gap with a dielectric constant of unity. Structures employing silicon on nothing (SON), having empty space beneath the top Si layer, have been also investigated. Trench structures with high aspect ratios formed by reactive ion etching were heat-treated in H_2, which resulted in the empty space in Si (ESS) due to silicon surface migration.[100] The desired shape and area of the ESS can be obtained depending on the size and layout of the initial trenches. A SON-MOS field effect transistor (MOSFET) was successfully fabricated using the ESS technique.

5.2 SiGe Wafers

It is well known that a biaxial tensile strain in Si reduces the intervalley scattering and lightens the effective mass by splitting the band degeneracy, which results in the enhancement of carrier mobilities. A biaxial strain is induced in a thin Si layer grown on a relaxed SiGe layer which is grown on Si substrate. For a high-quality Si/SiGe/Si structure, a SiGe buffer layer with a linearly graded Ge concentration profile[101] is greatly used, and a thin Si buffer layer grown at a low temperature reduces the dislocation density to as low as 10^4/cm^2 in mismatched SiGe/Si heterostructures.[102]

A commercially available strained Si wafer is fabricated by three steps; (1) growth of graded SiGe layer (3–4μm), (2) planarization and polishing, (3) growth of strained Si thin layer, of which the layers are grown by CVD.[103] It is reported that the thickness and uniformity of such strained Si layers is 17.5nm ±5% and their rms roughness after CMP is less than 2Å.

Recently, with respect to SiGe/SOI structures, much concern has arisen regarding the suppression of short channel effect and the reduction of junction capacitance with decreasing design rule. Various fabrication methods have been investigated. By means of the SIMOX technique using oxygen implantation at 25keV and annealing at 1280°C, $Si_{0.82}Ge_{0.18}$/SOI was successfully created.[104] In order to obtain an ultrathin SiGe/SOI with a higher Ge content, a condensation method was developed.[105] Graded SiGe and uniform $Si_{0.9}Ge_{0.1}$ layers grown on Si were implanted by oxygen followed by annealing for SIMOX structure. Finally, by oxidation at 1050°C below the melting point of the SiGe layer, an

ultrathin $Si_{0.43}Ge_{0.57}$/SOI with a Ge content was fabricated because the Ge atoms were condensed into the SiGe/SOI layer due to the rejection of Ge atoms from the oxide layer. Using the condensation method, in the SiGe/SOI with a Ge content of 25%, the electron mobility and hole mobility were enhanced by 1.85 times and 1.5 times compared with the universal mobilities, respectively.[106)]

6. Future Prospect and Issues

It is certain that silicon crystal is indispensable to ULSI as a basic material, and will continue to be used indefinitely. However, for the continuing and healthy growth of the silicon wafer industry, many issues have to be resolved. On the other hand, the fundamental research and development of innovative silicon wafer technologies are expected to satisfy the demands for a wide variety of leading-edge devices.

6.1 Silicon wafer industry

It seems that the requirement of the technology roadmap which covers the long-term-years is over-stringent. For example, the technical roadmap of the Semiconductor Industry Association (SIA) in 1994 indicated that SFQR would be 0.08μm and particle size ≧ 0.04μm for the 0.13μm design rule to be developed in 2004.[107)] In other words, SFQR and particle size which were 1/1.6 and 1/3 times of the design rule, respectively, were required. However, the actual specifications are more relaxed; The SFQR and particle size required are comparable to or less than and comparable to the design rule, respectively. It was reported that there is actually no difference in the final yield of 0.17μm DRAM between the "good" flatness wafers recommended by the ITRS and the "bad" ones.[108)] Furthermore, it is pointed out that the continuing tightening of material quality needs to be re-examined and re-looked at wafer requirements due to using innovative technologies and new process materials.[109)] The silicon wafer industry must make major investments at long periods in advance to achieve the development of technologies which can satisfy the severe technology roadmap requirements. Additionally, the severe specifications place much pressure on the manufacturing cost and also bring the waste of valuable resources.

It is of great importance for wafer manufacturers to establish a reproducible manufacturing technology which does not have fluctuation against the actual targets, although it must be important to achieve the stringent specifications with desperate effort. For this reason, active exchanges and a significant degree of reliance between device and wafer manufacturers are indispensable. It is recalled that in the early 1980s mutual information exchange and collaboration between these parties were promoted for the successful development and mass-production of DRAM, and fruitful results such as device yield improvement were obtained.

6.2 Choice and issues of current silicon wafers

A variety of silicon wafers have been developed and manufactured. Based on the understanding of grown-in defects and the precise control of crystal growth technology, "pure silicon wafer" has come into practical use. A MDZ wafer fabricated by RTP alone was developed. The issues of these polished wafers will be the cost reduction for 300mm. In order to be widely accepted by device makers, more than two suppliers will be necessary.

Regarding annealed wafers, the establishment of productivity for hydrogen annealed 300mm wafers and the migration of boron atoms to the surface due to hydrogen annealing as shown in Fig. 13 are the key issues. The most important problem associated with nitrogen doped wafers by annealing in Ar is the quantitative measurement of nitrogen concentration, particularly at values less than 1×10^{14} atoms/cm^3. The nitrogen concentration in Si wafer is calculated using the initial quantity of doping nitride and the conversion efficiency of nitrogen in Si. It is reported that the measurement down to 2×10^{14} atoms/cm^3 is possible by IR absorption, through using the sum of absorption by the interstitial N pair, N_2O and N_2O_2, and down to 4×10^{13} atoms/cm^3 by secondary ion mass spectroscopy (SIMS).[110)]

Recently, the small amount of nitrogen with a concentration of 3×10^{13} atoms/cm^3 was successfully measured in a nitrogen doped Si crystal by using a Fourier-transform infrared spectrometer (FTIR) at liquid He temperature using O–N–O complexes, which were found to be solely dominant for the nitrogen concentrations less than 1×10^{14} atoms/cm^3.[111)] The further improvement and the practical use of this method are expected. For mass production, it is convenient that a nondestructive measurement technique using FTIR at room temperature similar to oxygen is used.

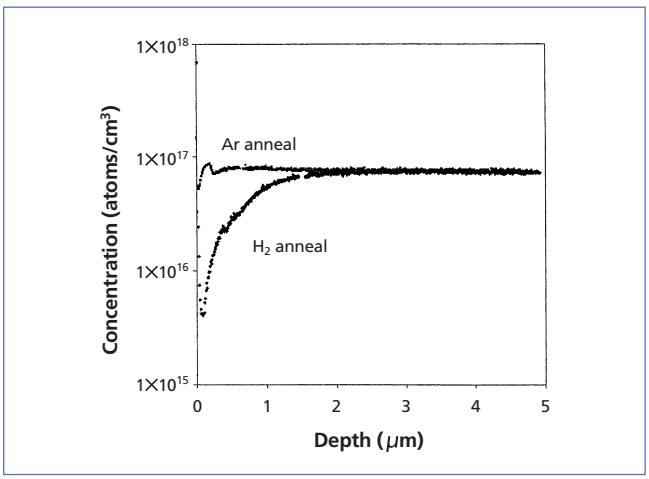

Fig.13. Depth profiles of boron concentration after annealing in Ar and H_2 at 1200°C for 1h.

The choice of epitaxial wafers, p/p$^-$ or p/p$^+$, compared to mirror-polished or annealed wafers, strongly depends on the device structures and the over-all total cost, including device process and wafer costs. Anyway, the cost reduction has to be proceeded. Recently, concepts for a low-price p/p$^-$ epitaxial wafer[112] and a high-quality epitaxial layer as thin as 0.5μm, using a very cost effective deposition scheme and substrates,[113] have been presented.

Whichever wafers are chosen to satisfy the stringent demands of various devices, economically reasonable prices have to be considered based on the cost effectiveness. It is sometimes experienced that those wafers which contribute to device yield improvement needs manufacturing extra cost. Reasonable price is necessary to maintain the coexistence of both device and wafer makers.

6.3 Challenge to innovative Si wafers

The development of SOI technology is steadily continuing and the mass-production line is being gradually strengthened. The next target is the establishment of a mass-production technology which achieves cost reduction. Recently, an interesting method for fabricating SOI structures which uses the implantation damage of light ions such as H$^+$ and He$^+$ has been proposed.[114] A slow ramping rate and a high oxygen concentration in the atmosphere for the annealing enabled the creation of a continuous BOX structure by forming oxygen precipitates. This technique is promising for the improvement of the quality of patterned SOI and SON structures due to low implantation damage.[115]

Bonding SOI offers the possibility of bonding with other materials. It is pointed out that XOI structures of which the active layers are SiGe, GaAs and SiC, and SOX structures of which the base materials are glass, sapphire, diamond, plastic and so on are possible.[116] A wide range of device applications is expected. The SOI structure with base metal material is promising for 10GHz operation and giga-scale integrated system LSIs,[117] which is fabricated using bonding technology.

Besides DRAM and the microprocessors (MPU) indicated by the technology roadmap, new silicon devices with various functions and unique performances are expected to contribute to the future development of the semiconductor industry. The innovative Si wafers to support those new devices are attractive. A one-chip CMOS with both an analog RF circuit and a large-scale digital circuit is required for wireless communication networks. For the system, high Q inductors and low-loss transmission lines are indispensable, and thus high-resistivity Si wafers above 2500Ω·cm are required.[118] Although high-resistivity wafers are easily available from FZ and MCZ wafers with low oxygen contents, CZ wafers are usable. It was demonstrated that by applying a multistep annealing from low to high temperatures, CZ wafers with initial oxygen contents of at least 15×10^{17} atoms/cm^3 with a conversion factor of 4.81×10^{17}/cm^2 are converted to have high resistivities of 1000Ω·cm and up without donor formation during device processing.[119]

Nitrogen doped Si wafers are expected for practical use. However, the physical phenomena of nitrogen in Si are not thoroughly understood. On the other hand, many spectroscopic data of hydrogen in Si have been well identified. For example, it is confirmed that the optical absorption peaks at 1987 and 1990cm^{-1}, 2122 and 2145cm^{-1}, and 2223cm^{-1} are due to IH_2, VH_2 and VH_4, respectively.[120] On the basis of the observation that in FZ crystal grown in H_2 followed by the slow cooling vacancy-hydrogen complexes, VH_4, do not grow into large clusters such as voids and swirls, Suezawa has proposed that high-quality COP-free Si crystals are hopefully grown in an atmosphere of H_2 and Ar with optimum percentage.[120] VH_4 complexes are observed to dissolve at around 600°C and come out of the wafer. Hydrogen in Si is worth investigating.

MOS devices have been fabricated using (100) substrates for a long time because of the many advantages. Recently, much attention has been paid to (113) and (110) substrates. High-quality SiO_2/Si (113) films can be produced by standard oxidation techniques, because Si (113) exhibits a significantly lower oxidation-induced roughening than Si (001).[121] The 110GHz cutoff frequency of the ultrathin gate oxide p-MOSFETs on the (110) substrate was demonstrated, because Gm of p-MOSFET on the (110) substrate is 1.9 times greater than that on the (100) substrate.[122] It is hoped that crystal growth technology along the desired axes is developed for the efficient wafer fabrication and material loss reduction.

With regard to wafer fabrication technologies, a number of advanced nanotechnologies, including newly designed machines which were developed for 400mm wafers[123] are expected to be used for the mass-production line of 300mm and smaller wafers in the near future. For future innovations, various basic works are under investigation.

7. Conclusion

As mentioned above, Si wafers have contributed to the development and mass production of silicon ULSI devices. If innovative and high-quality Si wafers were not being supplied timely, further progress in the silicon device industry would not be anticipated. It is noted that silicon technology is expected to continue to be the most powerful driver of the information age for at least the next 100 years.[124] Si wafers will continue to play a significant role as a key material indefinitely.

However, tremendous developments in silicon technology are leading to large increases in manufacturing cost. Thus, achieving cost reductions is now the most important issue and its resolution will enable the next stage of growth in the semiconductor industry. The reduction in cost of manufacturing is important, but breakthroughs in technology leading to cost reductions are also expected. From this point of view, mutual exchanges between science and technology with respect to silicon materials is earnestly desired.

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Hideki Tsuya was born in Hokkaido, Japan in 1938. He received his B.S. degree in Physics from the University of Tokyo in 1962. He joined NEC Co. Ltd., Central Research Laboratories in 1962. He earned his Ph. D. in Engineering from the University of Tokyo in 1976. He was promoted to General Manager of the VLSI Development Division in 1989 and was Research Fellow of the R&D Group in 1991. He joined Sumitomo Sitix Co. as Managing Director and General Manager of Silicon Technology R&D Center in 1995. He was appointed as Technology Director of Sumitomo Metal Industries Ltd. in 1998 and Corporate Auditor of Sumitomo Mitsubishi Silicon Co. in 2002 before retiring in 2003. He is an author and coauthor of more than 70 original papers and 34 patents. He was awarded the 39th Okochi Memorial Grand Prize in 1993. He served concurrently as Visiting Professor of North Carolina State University in 1993 and Kyushu University in 2000. He is a member of the Japan Society of Applied Physics.