GaAs-based high-frequency and high-speed devices

Masaaki KUZUHARA and Shinichi TANAKA

The explosive growth of new communication technologies such as the internet and mobile phones has expanded the applications of high-speed electronic devices based on compound semiconductors. In particular, the development of structures with superior electronic properties and advanced mass-production process technology has resulted in high-speed GaAs-based transistors that are making an important contribution to the improved performance of the latest mobile phone handsets and base stations. In this paper we describe how the technology behind such devices has developed so far, and outline the way in which GaAs-based high-speed electronic devices are currently implemented. Finally we review the prospects of cultivating new markets for such devices in the future.

Keywords: gallium arsenide transistor, high-power device, metal-semiconductor field-effect transistor, heterojunction field-effect transistor, heterojunction bipolar transistor, mobile communication, microwave, millimeter-wave

1. Introduction

High-speed electronic devices based on compound semiconductors are used in an ever-widening range of fields, such as amplifier devices in high-frequency radio equipment (e.g., mobile communication terminals) and switching elements in high-speed digital circuits. Among such devices, the best cost/performance ratios are achieved by GaAs-based transistors, which are establishing a firm position in the market for mass-produced devices that help to meet the needs of the modern telecommunication society. It is worthwhile studying how these devices have managed to attain such a status. There are at least two contributing factors, which are as follows:

The first is the inherent superiority of the electronic properties of GaAs materials. For the fabrication of high-speed electronic devices, these advantages include the following: 1) high electron mobility, 2) high electron drift velocity, 3) stable Schottky barrier height at room temperature, 4) the existence of thermally stable semi-insulating substrates, and 5) the ability to form a variety of heterojunctions on these materials.

Advantages 1) and 2) are the basic prerequisites for high-speed and high-frequency operation. In particular, in the latest devices for low-voltage mobile terminal applications, a competitive edge can often be obtained by reducing the parasitic resistance as much as possible. As a result, a high electron mobility is especially important.

Advantage 3) may seem rather mundane at first, but without a stable Schottky barrier height it would have been impossible to contemplate the development of the modern field-effect transistor (FET). Advantage 4)—the existence of thermally stable semi-insulating substrates—is a property that can be taken for granted with GaAs. However, silicon (Si) substrates do not exhibit this property, and at present it is only possible to provide them with equivalent characteristics through the use of advanced process technologies such as SIMOX (Separation by Implanted OXygen). In this respect it seems that GaAs materials are far better suited to high-frequency applications. Advantage 5)—the ability to form a variety of heterojunctions—provides designers with a greater degree of latitude in the types and combinations of materials that can be used to configure devices. This facilitates the development of GaAs device families tailored to the requirements of a diverse range of products with different functions. Heterojunctions that can typically be formed on GaAs substrates include AlGaAs/GaAs and InGaP/GaAs.

The second factor is the solid progress that has been made by industrial process technology. Process technology can be broadly classified into crystal *growth* technology and material *processing* technology. With regard to the former, it is impossible to ignore the progress made in the use of larger wafer sizes on GaAs single-crystal substrates. The standard diameter of GaAs wafers is currently changing from four to six inches. To accommodate this increased substrate size, epitaxial growth techniques are also being developed for processing multiple 6-inch wafers simultaneously, and it is also becoming possible to control layer thicknesses to within 1 nm.

On the other hand, in material processing technology, dry-etching techniques are being developed with superior reproducibility and uniformity and with low damage by combining anisotropic etching with the selective etching properties of heterojunction materials. The use of heterojunctions is important, not only for obtaining new functions from their physical properties but also because they provide a means of improving the dimensional controllability of crystal processing. The secret to success in the mass production of high-performance devices is hidden in the properties of heterojunctions.

In this paper we will describe the transitions that have so far been made in the technology and the current status of its implementation, with particular reference to mobile communication applications and GaAs-based high-speed electronic devices. We will also describe the latest techniques that are currently under development. We will then describe the development trends in device technology for third-generation (3G) mobile phones—for which services were started in 2001—by focusing separately on their application to mobile terminals and base stations. Finally, we will describe some other potential applications for this technology be-

Photonic and Wireless Devices Research Laboratories, NEC Corporation (2-9-1 Seiran, Otsu 520-0833)
e-mail : kuzuhara@bu.jp.nec.com

sides mobile communications.

2. Application to Mobile Phone Terminals

2.1 Field-effect transistors

2.1.1 Double-doped/double hetero structures

Over the last few years, mobile phone terminals have evolved into pocket-sized devices weighing no more than 100 g and occupying no more than 100 cm^3. This level of miniaturization has been achieved by reducing the voltage of the battery power sources. Until the mid-1990s, mobile phones were operated either at 5.8 V (five nickel-cadmium (NiCd) or nickel monohydride (NiMH) cells) or at 4.6 V (four of these cells instead of five), but due to the wide availability of lithium ion secondary cells and the development of power transistors capable of operating with a 3 V supply, the use of 3 V power sources has now become the *de facto* industry standard. Also, since transistors have been developed with structures that make them suitable for high-efficiency operation, subsequent technical reforms have made it possible to achieve substantial improvements to the talk time and standby time.

But to produce power transistors capable of delivering output signals of the order of one watt, the switch to low-voltage 3 V power sources means that these devices must be operated with higher currents than before. The Japanese domestic technical standard for personal digital cellular communication (PDC) requires mobile phone terminals to produce a microwave output power of at least 1 W. According to simple AC theory, the current drawn by the transistor is about 1.3 A for a 3 V bias if the transistor's internal resistance (on-resistance) is ignored. In practice, since the presence of on-resistance further reduces the amplifier's power conversion efficiency, the required current is even higher.

With the aim of achieving optimal operation with a 3 V supply, we first looked into increasing the maximum drain current density per millimeter of gate width in the FETs. For this purpose it is effective to increase the electron density present in the FET channel. However, in a conventional MES (metal–semiconductor) FET structure, increasing the concentration of impurities in the channel layer causes a large negative shift in the threshold voltage and a sharp drop in the gate breakdown voltage. A large negative shift of the threshold voltage may result in a gate bias of -3V or less, which is inconvenient to prepare when operating with a 3 V supply. Also, even when operating at 3 V, a gate breakdown voltage of at least 10 V is generally required for stable operation, and conventional MES structures are limited in this respect.

On the other hand, with heterojunction FETs it is possible to increase the drain current without causing much change to the threshold voltage or gate breakdown voltage. The optimal structure for meeting this requirement is a double-doped/double heterostructure.[1,2] This structure is characterized by having a channel layer of GaAs or InGaAs sandwiched between layers of n-AlGaAs situated above and below it. By striking a design balance between the upper and lower doped layers, the gate breakdown voltage and the maximum drain current can be controlled independently.

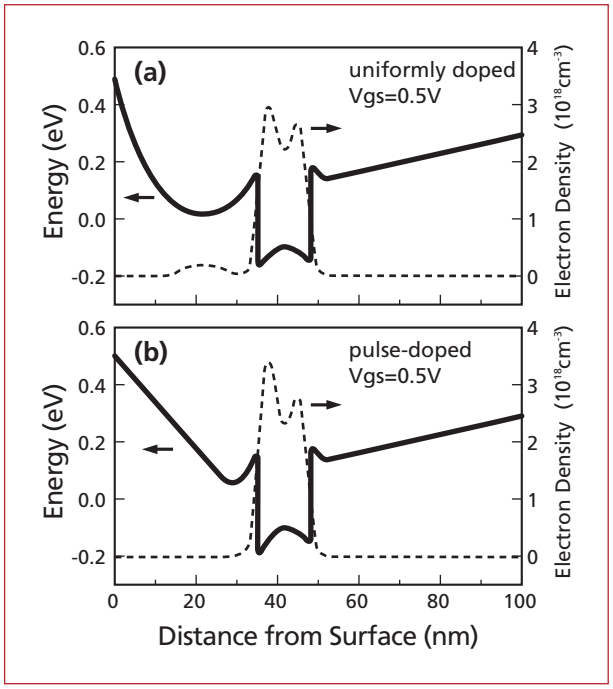

Fig. 1: The distribution of conduction band energy and electron concentration across double-doped/double heterojunctions. (a) Uniformly doped structure. (b) Pulse-doped structure. In the uniformly doped structure, it can be seen that electrons spread out into the AlGaAs electron supply layer.

Figures 1(a) and 1(b) show the conduction band energy distribution and electron density distribution in two types of double-doped/double heterostructure. In the uniformly doped structure (Fig. 1(a)), a gate electrode directly contacts with an n-AlGaAs Schottky layer doped uniformly with impurities (e.g., n=1.0×10^{18} cm^{-3}, thickness 34 nm). On the other hand, in the pulse-doped structure (Fig. 1(b)), there is a thin layer of n-AlGaAs doped with a high concentration of n-type impurities (e.g., n=4.5×10^{18} cm^{-3}, thickness 9 nm) below an undoped AlGaAs Schottky layer (e.g., thickness 26 nm).

2.1.2 Depletion-type heterojunction FETs

The results of evaluating the DC and high-frequency characteristics of prototypes of the abovementioned two types of heterojunction FET (gate length 1.1 μm) were presented in an earlier report.[3]

With a pulse-doped structure it was possible to obtain a gate breakdown voltage 3 –4 V higher than that of a uniformly doped structure, and a saturation-drain voltage (knee voltage) about 0.10–0.15 V lower. These benefits are due to the use of an undoped AlGaAs Schottky layer at the surface, whereby 1) the injection of electrons from the gate metal to the semiconductor is suppressed, and 2) the parasitic parallel conduction of electrons in the AlGaAs layer (parasitic MESFET effect) is suppressed.

When an FET with a pulse-doped structure was used for power amplification (AB-class operation) at 950 MHz with a 3 V power supply, it was found to have a saturated output power of 1.4 W, a power-added efficiency of 60%, and a linear gain of 12.7 dB.[3] This report was the first to demonstrate the benefits of using double-doped/double heterojunction FETs as power amplifier transistors that operate efficiently at low voltages.

In 1993, analog mobile phone systems began to be replaced by digital systems that are sensitive to waveform distortion. To satisfy Japan's domestic PDC technical standard with a 3 V power supply, it is thus necessary to achieve an output of 1 W in the linear operating region of the FET, as opposed to analog phones which used amplification in the saturated region. Also, to extend the phone' s talk time it is also important to improve the power conversion efficiency (i.e., the power-

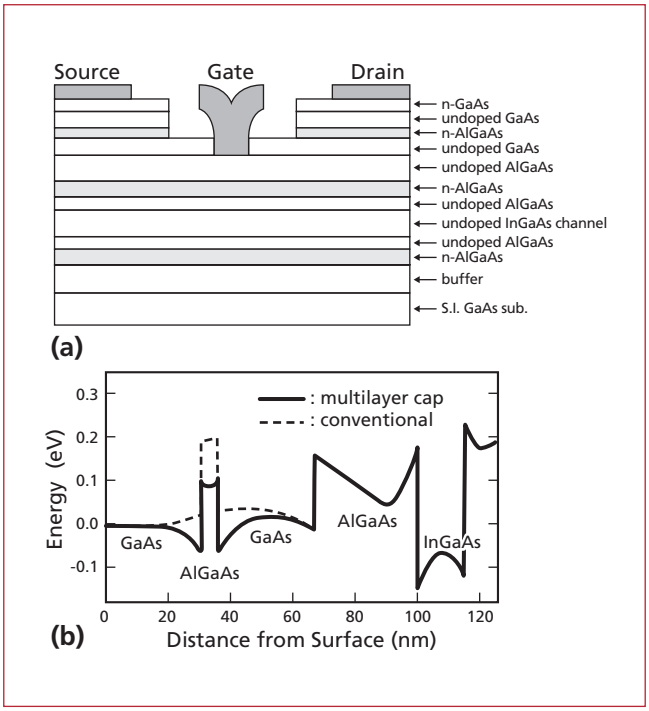

Fig. 2: A heterojunction FET with a multilayer cap structure. (a) Cross-sectional structure. (b) Conduction band energy distribution under the ohmic electrode. The use of a multilayer cap structure reduces the potential barrier at the n-AlGaAs layer near the surface.

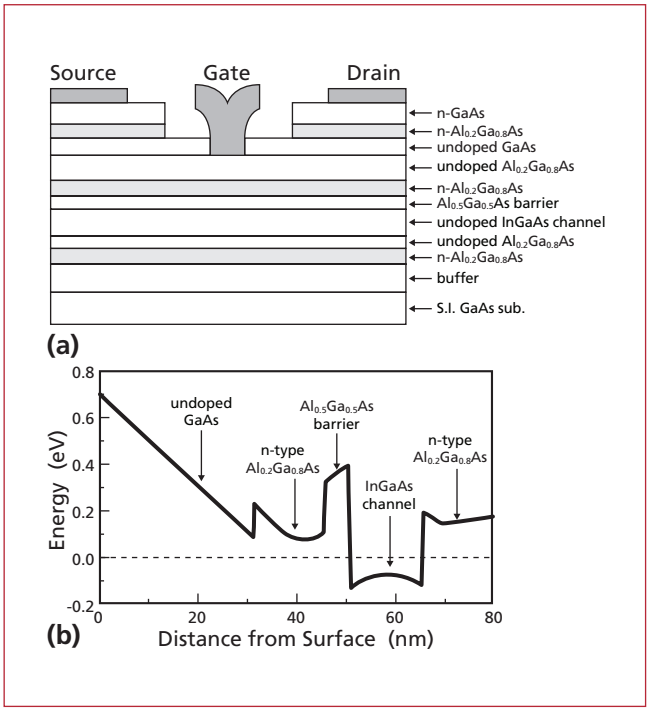

Fig. 3: A heterojunction FET with an $Al_{0.5}Ga_{0.5}As$ barrier layer. (a) Cross-sectional structure. (b) Conduction band energy distribution under the gate electrode. The introduction of a barrier layer suppresses the injection of electrons from the channel towards the gate electrode.

added efficiency), and to reduce the FET's knee voltage (i.e., reduce the on resistance). Furthermore, it should be possible to mass produce these devices with high yield, and with small chip dimensions.

To satisfy these requirements, the gate length was reduced to 0.8 μm and a two-stage recess embedded structure was employed for the gate electrode (see Figs. 2 and 3 below).[4] As a result, the drain current density was increased to 600 mA/mm (about 1.5 –2 times higher than a conventional device), and the on-resistance was reduced to 2.3 Ω·mm. Selective dry etching of AlGaAs and GaAs was used to form the two-stage recess, and the variation of recess etching depth across the wafer was kept to a minimum by using the former as an etching stop layer.

The large-signal characteristics of this improved FET were measured with a 950 MHz QPSK (quadrature phase shift keying) digitally modulated signal.[4] In a miniature chip with a gate width of 7 mm, a power-added efficiency of 56.3% was achieved with an output power of 1.23 W when operated at 3.4 V.

2.1.3 Enhancement-type heterojunction FETs

The heterojunction FETs introduced so far have all been depletion-type devices with negative threshold voltages. A drawback of this type of device is that two power supplies—one positive, the other negative—are needed to achieve amplification. Since Si-MOSFETs and bipolar transistors (described below) can operate with a single power supply, the fact that twin positive and negative power supplies are only needed for heterojunction FETs is a distinct disadvantage. To reduce the number of circuit components and develop products that are more compact and less expensive, it is desirable to develop enhancement-type heterojunction FETs that have a positive threshold voltage and can be operated with a single power supply. However, enhancement-type FETs have generally suffered from reduced maximum drain current and increased on resistance, leading to reduced power density and efficiency.

To address the abovementioned problems of enhancement-type FETs, a new multilayer cap structure was introduced.[5] Figure 2(a) shows the cross-sectional structure of this FET, and Fig. 2(b) shows the conduction band energy distribution below the ohmic electrodes. In this structure, an undoped GaAs layer and a heavily-doped n-AlGaAs layer are deposited in turn below the heavily-doped n-GaAs layer in contact with the ohmic electrodes. Since a two-dimensional electron gas is formed in the GaAs layers in contact with both sides of the abovementioned heavily-doped n-AlGaAs layer, there is a smaller potential barrier at the n-AlGaAs layer that also serves as an etching auto-stop layer. This effect makes it possible to reduce the contact resistance along the path from the heavily-doped n-GaAs surface layer to the InGaAs channel layer.

Tests were performed on an experimental enhancement-type heterojunction FET with a gate length of 0.5 μm and a multilayer cap structure.[5] When a threshold voltage of +0.20 V was selected, a large maximum drain current density of 390 mA/mm was achieved, and the device also exhibited a large gate breakdown voltage of 17 V. By employing a multilayer cap structure, the parasitic resistance could be reduced by 0.1 Ω·mm and it was possible to obtain an on-resistance of 1.6 Ω·mm.

For an FET with a gate width of 24 mm, as a result of evaluating the power characteristics with a single 3.5 V power supply, an output power of 1.0 W and a power-added efficiency of 65.5% were achieved—enough to satisfy the PDC technical standard. In this device, it was also possible to cut off the drain current to just 2 μA/mm just by setting

the gate voltage to 0 V. Consequently, there was no need to turn off the drain supply by providing a separate switch circuit. In other words, use of an enhancement-type FET makes it possible to eliminate not only the negative power supply circuits but also the drain bias switching circuits from the mobile phone terminals.

In an enhancement-type FET, as the difference between the threshold voltage and the gate forward on voltage (V_F) decreases, it becomes harder to maintain a large maximum drain current. Also, during power operation a forward gate current flows more readily, increasing the likelihood of the amplifier operation becoming unstable. Accordingly, it becomes necessary to increase V_F.

Figure 3(a) shows the cross-sectional structure of an enhancement-type heterojunction FET developed for this purpose, and Fig. 3(b) shows the conduction band energy distribution under the gate electrode.[6] This differs from a conventional structure in that an $Al_{0.5}Ga_{0.5}As$ barrier layer (0.5 nm thick) with a large bandgap energy is inserted between the InGaAs channel layer and the upper n-AlGaAs electron supply layer. By employing this new structure, it is possible to achieve an equivalent increase of V_F while avoiding the injection of electrons traveling from the channel toward the gate electrode when a positive gate bias is applied.

Figures 4(a) and (b) show the drain current vs. voltage characteristic and the gate forward characteristic of an enhancement-type FET having an $Al_{0.5}Ga_{0.5}As$ barrier layer (gate length 0.5 μm). The maximum drain current density was 370 mA/mm, and the threshold voltage was +0.17 V. The value of V_F determined from the gate forward current vs. voltage characteristic is 0.9 V, which represents an improvement of 0.2 V compared to the device with no $Al_{0.5}Ga_{0.5}As$ barrier layer.

For an enhancement-type FET with a high V_F of this sort (gate width 16 mm), the input/output power characteristics were evaluated with an input signal consisting of a 1.95 GHz digital phase-modulated signal diffused at a chip rate of 3.86 Mcps according to a W-CDMA (wideband code division multiple access) scheme. By adjusting the input and output matching circuits to maximize efficiency while suppressing power leakage to an adjacent channel (separated by 5 MHz) to -35 dBc or less, the following favorable results were obtained when operating the device with a single 3.5 V supply: output power 460 mW, power-added efficiency 58.9%, associated gain 12.6 dB. Moreover, the gate leakage current during peak output was only 0.8 μA, thus verifying the effect of introducing the barrier layer.

In a W-CDMA scheme, the transmitted power strength of the terminal side is controlled over a wide range according to the distance from the base station. When the amplifier is biased under class A or class B operation, the efficiency generally becomes worse as the output power is reduced from the saturated output point.

A method proposed for avoiding this problem involves using a DC-DC voltage converter to dynamically control the drain bias voltage V_{ds}.[7] It has been reported that this method allows the power-added efficiency of the amplifier to be increased from 8% (V_{ds} = 3.5 V) to 21% (V_{ds} = 1.0 V) when the output power is 20 mW. Here, it was possible to achieve normal amplifier operation even when V_{ds} was reduced to 1.0 V because a double-doped/double heterojunction FET has a sufficiently low knee voltage. In practice, in a heterojunction FET with a gate width of 28 mm where the on-resistance is reduced to 1.3 Ω·mm, an output power of 1.0 W and a power-added efficiency of 59% have been achieved with a low bias voltage of 1.0 V.[8]

2.2 Bipolar transistors

The heterojunction bipolar transistor (HBT) is widely recognized as a mass-produced device that brings important benefits, especially to applications such as power amplifier elements in mobile phone terminals. Factors that have led to the growth in popularity of these devices include the fact that they help to make mobile terminals more compact and light-weighted because they can be driven by a single positive power source, and the fact that they are suitable for communication applications involving digital modulation schemes where linear operation is required because they have comparatively low distortion when operating with a large output signal.

Although AlGaAs has for a long time been used as a wide bandgap emitter material, the fact that InGaP and GaAs allow selective etching has recently resulted in a preference for the latter, which is more suitable for mass production. It is also apparent that the characteristics of the InGaP/GaAs heterojunction interface substantially improve the reliability of HBTs.[9]

There are two factors that can be said to contribute to the improved reliability associated with introducing an InGaP/GaAs heterojunction. First, since the density of defect levels at the InGaP/GaAs interface is lower than in the case of an AlGaAs/GaAs interface, it has the effect of reducing the recombination current arising from defect levels that contributes to the device lifetime. Secondly, since the difference in bandgap energy that occurs between the InGaP and GaAs (about 0.5 eV) mostly appears as a discontinuity in the va-

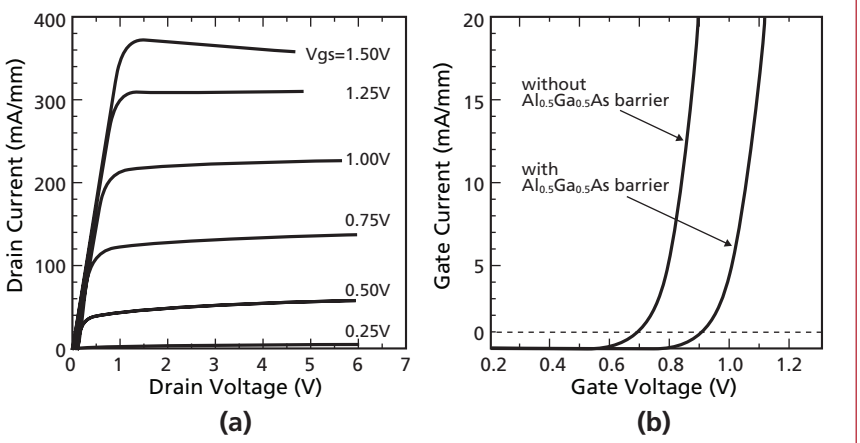

Fig. 4: (a) Drain current vs. voltage characteristics and (b) gate forward characteristics of an enhancement-type heterojunction FET with an $Al_{0.5}Ga_{0.5}As$ barrier layer. The introduction of a barrier layer improves the forward on voltage by about 0.2 V.

lence band, it has the effect of suppressing the recombination current that arises from the reverse injection of holes in the base layer into the emitter.

It has recently been estimated that an InGaP/GaAs HBT with a junction temperature of 135°C has a very long lifetime of 3.6×10^8 hours,[10] making HBTs essential for mobile terminal applications where high reliability is required.

Studies are being made of how to improve the materials used in GaAs-based HBTs, not only to make them easier to mass produce and more reliable, but also to enhance their performance. As in the case of heterojunction FETs, a wider range of device possibilities can be made available if the lattice matching constraints can be relaxed. An example of this is the drift base HBT, which uses a layer of $In_xGa_{1-x}As$ with a ramped composition (see Fig. 5). This HBT structure can improve the current gain blocking frequency without producing dislocations or defects, even when a strained layer is introduced into the device.[11]

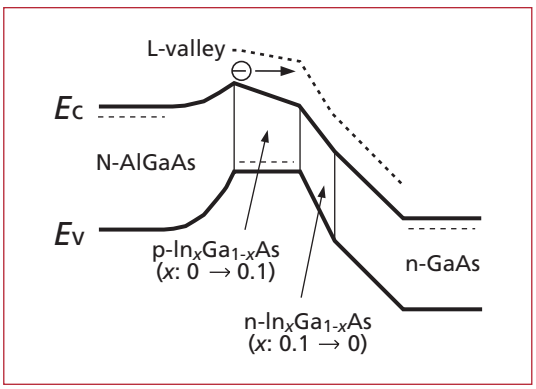

Fig. 5: Energy band diagram of a drift base HBT incorporating a layer of $In_xGa_{1-x}As$ with a ramped composition.

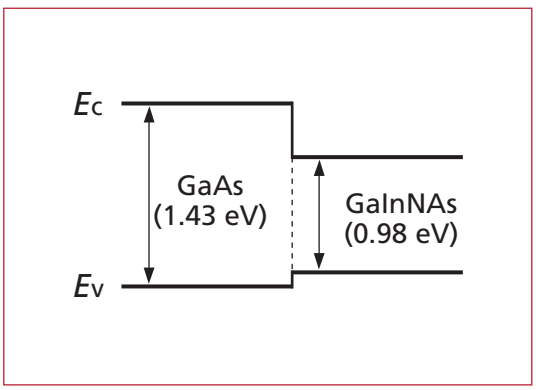

Fig. 6: Relationship between the band positions in GaAs and GaInNAs. Most of the difference in bandgap energy appears as an energy discontinuity at the conduction band side.

The advantages of a drift base HBT include: 1) a larger average drift velocity for electrons in a given accelerating field due to the ability to maintain a large conduction band energy difference between the Γ and L valleys, and 2) the absence of Al exposed at the surface where it can interfere with the formation of external base layer electrodes.

Adding In to the GaAs is preferable in that it makes the bandgap in the base layer narrower and reduces the operating threshold voltage. However, since lattice mismatch problems may arise, there is a limit to the amount of In that can be added. Attention has thus recently turned to GaInNAs compositions where small quantities of nitrogen are added to the InGaAs, resulting in powerful materials that can be used to make HBTs that operate at lower voltages while maintaining lattice matching with the GaAs. Figure 6 shows the relationship between the band positions in GaAs and GaInNAs. A problem to be addressed with this technique is that when GaInNAs and GaAs form a heterojunction, most of the difference in bandgap energy appears as an energy discontinuity on the conduction band side.[12]

The abovementioned result shows that a GaInNAs base structure is ideal for pnp transistors, but is not suited for npn transistors as it is because it produces a potential barrier to electrons. An example has been reported in which a GaAs/GaInNAs chirp superlattice is employed to achieve excellent npn operation.[13] In this example, an artificial ramped composition layer is formed by the superlattice, and the small bandgap of the $Ga_{0.89}In_{0.11}N_{0.02}As_{0.98}$ base layer (0.98 eV) is effectively linked to the reduction of the threshold voltage. However, there are still problems associated with the crystal quality and doping concentration in npn HBT base materials, and further remedial studies should be carried out to achieve a high current gain combined with a low base resistance.

As described above, GaAs-based HBTs are expected to open up new possibilities in the future through the introduction of new materials and heterojunctions incorporating these materials. The ability of HBTs to operate from a single power source and their high power densities are significant advantages over FET devices, but there are still several problems that need to be addressed, such as the existence of offset voltages in the collector characteristics, achieving uniform-temperature operation across a chip, dealing with thermal runaway, and coping with surges and load fluctuations. It will be a while yet before these problems are fully addressed. In the market for mobile terminal products, it is worthwhile predicting how the market share of FETs and HBTs will change in the future, but for HBTs it is vital to have a comprehensive debate at least including the problems mentioned above.

3. Application to Mobile Phone Base Stations

3.1 Current status of microwave transistors for base station transmitters

The main purpose of a mobile phone base station is to relay voice and data communications over radio channels while updating the positional information relating to mobile terminals that are constantly on the move. According to figures gathered in September 2001, some 65 million mobile terminal contracts have been registered in Japan, and the number of base stations that have been built across the country to accommodate these users is already in excess of 33 thousand.[14]

To accommodate the recent explosive growth in the number of mobile phone terminals, the number of communication channels needs to be increased. For this purpose, a transition is under way towards third-generation (3G) mobile phone systems that use bandwidth more efficiently. At the same time, to increase the volume of traffic that can be carried in each base station area, increasing the output power of microwave signals transmitted from the base station antennas is also an important issue. In particular, in current systems where a single amplifier is used to amplify multiple carrier waves at the same time, it is necessary to cope with instantaneous peak outputs approximately an order of magnitude larger than the average output power so that the transmitter amplifier becomes never saturated. This is referred to as operating the power amplifier with back-off,

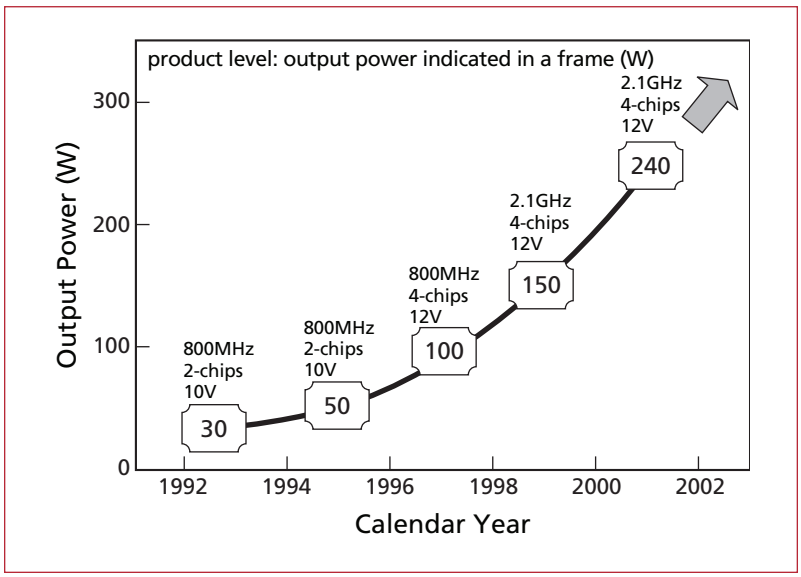

Fig. 7: The year-on-year growth in the performance of high output GaAs FETs developed for mobile phone base stations.

and allows high-quality digital radio communication to be achieved with a low bit error rate. For these reasons, there is currently a strong need for increased output power from the microwave transistors used in base station transmitters.

FETs based on GaAs and Si semiconductors have been widely used in the transmission power amplifiers of mobile phone base stations. The former have better high-frequency characteristics but have a serious drawback with respect to high voltage operation. On the other hand, although the latter can be successfully operated at voltages as high as 20–30 V, it is hard to achieve favorable high-frequency characteristics. In terms of cost, Si-based FETs are much less expensive, but 3G mobile phones—which are expected to become widespread in the future—use the 2 GHz band which is higher than the frequency of conventional systems. Accordingly, the current status is that the better high-frequency characteristics of GaAs FETs give them the advantage in terms of overall performance.

At the product level, let's see how increases have so far been made to the output power of high-power GaAs FETs. Figure 7 shows the year-on-year growth in the performance of high-power GaAs FETs developed for mobile phone base stations. Since 1997, when the 100 W barrier was broken for the first time by mounting four FET chips in a single package, there has been steady growth in the output power available from such devices. According to the latest data, there are reports of 240 W products being available on the market, and 300 W devices have already been produced in the laboratory.[15)]

Power supply voltages have remained fixed at 10–12 V throughout this period, so the output power levels attained so far have all been achieved by increasing the drain current. Although this can be done by using larger transistor chips or greater numbers of chips, there are a number of accompanying problems that are exacerbated by this approach.

First, there are limits to how large the chips can be made. The package dimensions are also limited, so it will become increasingly difficult to carry on increasing the chip size in the future. Another problem is that increased output current is associated with reduced input impedance. Since matching circuits with a large impedance conversion ratio add to the complexity, this aggravates problems such as increased reflection loss and bandwidth reduction. Finally, there is the problem that larger power supply circuits generate more heat. Since the losses in a power supply circuit rise in proportion to the square of the current, this makes it harder to achieve energy savings at the base stations. As a result, the use of higher drain currents is no longer an ideal solution for achieving higher output power levels.

3.2 Heterojunction FETs with field plates

An attempt has been made to improve the operating voltage of GaAs FETs to 20 V or more, which is twice the normal voltage for such devices.[16)] This involved the use of a heterojunction FET with a new structure where a field plate (FP) connected to the gate electrode is situated on the surface passivation film between the gate and drain.

The cross-sectional structure of this FP-FET is shown in Fig. 8. The gate is formed on an n-AlGaAs surface layer, and controls the concentration of electrons in the n-GaAs channel layer below it. The FP electrode plays two primary roles. One is to moderate the electric-field strength at the drain end of the gate when the gate is subjected to a large negative bias when operating with large AC signals. It achieves this by depleting the channel layer underneath the negatively charged FP electrode, and as a result the gate breakdown voltage is substantially improved. The second role is to facilitate the flow of large AC drain currents, since the depletion layer in the channel under the FP electrode is instantaneously reduced when the gate bias swings in the positive direction. This has the effect of improving the linearity of the input/output power characteristics and allowing a large saturated output power to be obtained.

An experimental heterojunction FET with an FP electrode (gate length 1.0 μm, FP

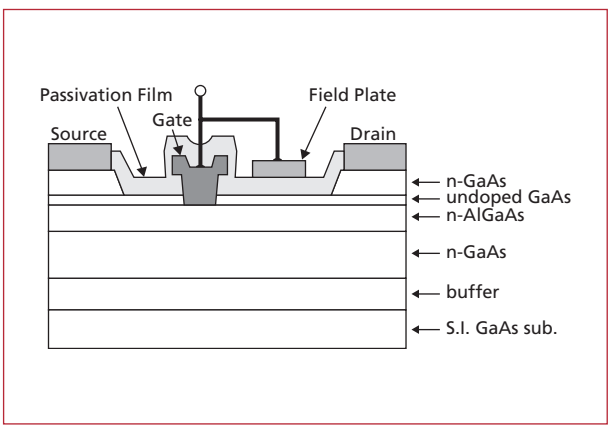

Fig. 8: Cross-sectional structure of a new type of heterojunction FET incorporating a field plate. The field plate is connected to the same potential as the gate electrode.

length 0.5 μm) has exhibited a peak drain current of 300 mA/mm and a gate breakdown voltage of 45 V. Figure 9(a) shows a photograph of an FET chip with a multi-cell structure designed for high power applications, and Fig. 9(b) shows a photograph of an FET amplifier with a partial matching circuit for push-pull operation that incorporates four of these chips. Each FET chip has a total of 108 gate fingers in a parallel arrangement, and the overall gate width is 86.4 mm. The chip measures 1.5 mm × 4.4 mm.

The output power of the push-pull amplifier was evaluated at 2.1 GHz, and was found to increase linearly as the drain voltage increased. At a drain voltage of 22 V, this device delivered an output power of 230 W with a power-added efficiency of 42% and a linear gain of 11 dB. A W-CDMA signal was input to this push-pull amplifier, and the leakage into a neighboring channel separated by 5 MHz was measured. As a result, the power leakage at an output power of 40 W (8 dB back-off point) was found to be –35 dBc or less, with a 25% power-added efficiency. The distortion characteristics at the back-off point were improved by about 4 dB due to the increased drain voltage, and it was verified that this device exhibits not only high output power but also low distortion when operated at high voltages.

Although these results were obtained with an experimental FP-FET with a GaAs channel, the fabrication of an FP-FET with an InGaP channel was also recently reported.[17] Such devices will allow base stations to operate at even higher voltages.

4. The Progress Toward New Applications

As the internet continues to grow, the data transfer speeds that networks are required to support are increasing rapidly. For wireless networks, a peak transfer speed of 54 Mbit/s has been achieved in 5 GHz band wireless systems such as HiperLAN/2 and IEEE802.11a, which are currently being standardized.[18] However, cable-based systems are progressing at an even faster rate. Accordingly, even in wireless systems it is expected that gigabit wireless communications will appear for applications such as real-time video streaming and high-speed downloading.

Since August 2000, the 60 GHz band (59–66 GHz) has been released for the operation of license-free wireless systems, and it is strongly anticipated that this band will be used for wireless systems operating at 100 Mbit/s and above. For example, an experimental miniature transceiver module for the 60 GHz band has been configured by flip-chip mounting a coplanar MMIC (monolithic microwave integrated circuit) consisting of 0.15 μm gate GaAs heterojunction FETs onto a multilayer glass ceramic substrate.[19]

Figure 10 shows a photograph of the transmitter and receiver modules. The transmitter module incorporates three types of MMIC—a 30/60 GHz frequency multiplier, a modulator and a transmitter amplifier—and the receiver module incorporates two types of MMIC—a low-noise amplifier and a demodulator. This 60 GHz band transceiver module was used to build a prototype two-way radio transceiver conforming to IEEE 1394, and was able to operate at 500 Mbit/s with an ASK (amplitude modulation) scheme.

Oscillators are essential components of millimeter-wave systems of this sort. HBTs are suitable for oscillator applications because these devices have a vertical configuration. This means that they are affected little by 1/f noise sources located at the semiconductor surfaces, and as a result they exhibit significantly low phase noise (fluctuation of the oscillator frequency)—which is one of the most important factors determining the performance of an oscillator. Figure 11 shows the surface appearance of an experimental 38 GHz band MMIC oscillator chip which uses

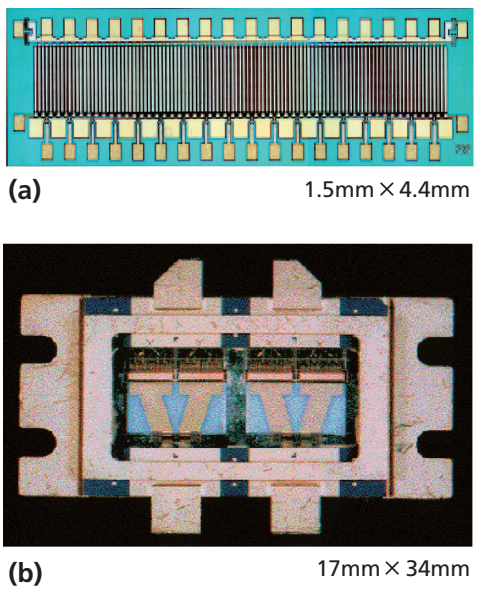

Fig. 9: Heterojunction FETs with field plates. (a) Photograph of a chip with a multi-cell structure consisting of a heterojunction FET chip with field plates (chip dimensions: 1.5 mm × 4.4 mm). (b) Surface photograph of an amplifier with a partial matching circuit that incorporates four FET chips in the same package.

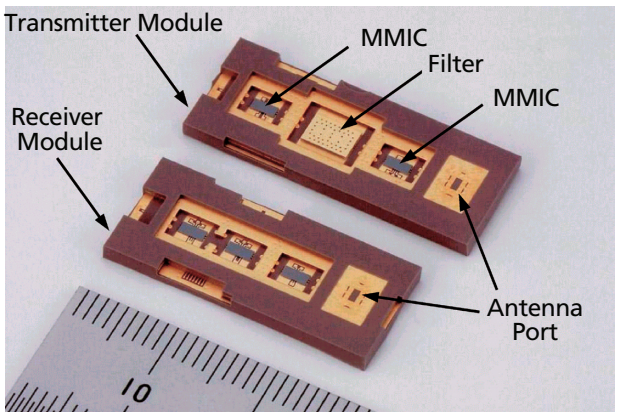

Fig.10: Photograph of miniature 60 GHz band transceiver modules. The transmitter module incorporates three types of MMIC—a frequency multiplier, a modulator and a transmitter amplifier. The receiver module incorporates two types of MMIC—a low-noise amplifier and a demodulator—and a bandpass planar filter.

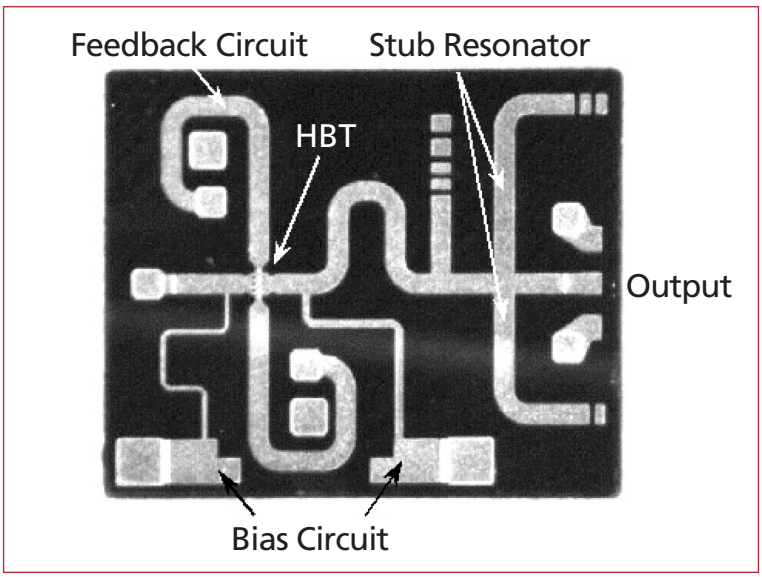

Fig. 11: A 38 GHz MMIC oscillator. An HBT with a graded composition InGaAs base structure is used as the active element. When detuned by 1 MHz, this oscillator has a favorable phase noise of –114 dBc/Hz.

an HBT with an InGaAs graded composition base structure.

5. Conclusion

Although GaAs is a semiconductor material with some favorable electronic properties, this does not mean that it has outstanding qualities. Its mobility is inferior to that of InGaAs, and its peak drift velocity is less than that of InP. Its bandgap energy is larger than that of Si, but much smaller than those of SiC or GaN. However, its overall performance makes it one of the best candidates for use in high-frequency devices. The successful use of GaAs in power amplifier devices for mobile phone terminals is also due to its overall superiority over other materials rather than the overwhelming benefits of any particular characteristic. Hopefully this paper has helped to convey this situation to some extent.

Although there is not enough space for this article to offer many specific examples of GaAs-based high-speed electronic devices, there will be an abundance of new applications for such devices in the future. It has been decided that specific frequency bands between 20 and 40 GHz will be used for high-speed wireless internet access technologies to complement ADSL (Asymmetric Digital Subscriber Line) and FTTH (Fiber To The Home). GaAs will probably play an important role in the wireless devices used for these applications.

As mentioned in this paper, GaAs devices are also being used for the initial prototypes of 60 GHz band millimeter-wave wireless systems. There is no doubt that GaAs—which has the longest history of all group III-V semiconductors—will continue to be used as the central material in high-speed transistors across a wide range of frequency bands while keeping other new semiconductor materials at bay.

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Masaaki Kuzuhara (D. Eng.)
Completed a Master's course in engineering at Kyoto University in 1981. Since joining NEC Corporation, he has been involved in the R&D of ion implantation in compound semiconductors, Monte Carlo simulation of compound semiconductors, compound semiconductor heterojunction devices and MMICs. From 1987 to 1988 he was a guest researcher at the University of Illinois.

Shinichi Tanaka (D. Eng.)
Completed a Master's course in engineering at the University of Tokyo in 1986. Since joining NEC Corporation he has been involved in the R&D of heterojunction bipolar transistors and MMICs. From 1992 to 1993 he was a guest researcher at Purdue University.