Conference Report

Report on the 2001 Symposium on VLSI Technology

Toshihiro Sugii

The 2001 Symposium on VLSI Technology was held from June 12th - 14th in Kyoto, Japan. Kyoto is the ancient capital of Japan. The capital was located there for over a thousand years, between 794 through 1868, before being transferred to Tokyo. Kyoto has many historic and scenic sites. However, it is not only a tourist attraction. It is also the home of many high-tech companies, which makes it an appropriate venue for presenting the latest R&D results in the area of VLSI technology.

The symposium catered to specialists in a range of VLSI technology fields, such as CMOS front-end technology, DRAM technology, advanced lithography, RF & analog device technology, nonvolatile memory technology, multilevel interconnect, and integration. The symposium had two invited plenary talks. One was "Manufacturing in 21st Century-New Concept for 300mm Fab" by Dr. Koike from Trecenti Technologies, Inc, and the other was "Design Technology for Systems on a Chip" by Dr. Camposano from Synopsys, Inc. Sixty-nine contributed papers were presented in parallel, and ramp sessions were held on the second night.

After the plenary talks, a highlight session was held in which this year's five most significant papers were presented. The first paper was "Highly Manufacturable and High Performance SDR/DDR 4Gb DRAM" by Samsung Electronics Corporation. A 4-Gb SDR/DDR DRAM was fabricated with 0.11-um CMOS technology. This was the first working DRAM of such high density ever achieved. The cell size and the chip size were 0.1 um^2 and 645 mm^2, respectively. The second paper was "Scaling Towards 35 nm Gate Length CMOS" by Advanced Micro-Devices, Inc.. Thirty-five-nm gate length planar CMOS transistors with aggressively scaled gate equivalent oxide thickness (EOT) were presented. A nitride/oxynitride stack was used as gate dielectric with EOT ranging from 1.2 nm down to 0.7 nm. The third paper was "A High Performance 100 nm Generation SOC Technology for High Density Embedded Memory and Mixed Signal LSIs" by Toshiba Corporation. The paper demonstrated a 100-nm-generation SOC technology for the first time. Three types of core devices (high performance, standard, mobile) were presented with optimized gate oxynitrides for their stand-by power conditions. This advanced LOGIC process is compatible with 0.18 um^2 trench capacitor DRAM and 1.25 um^2 6-Tr. SRAM. Two kinds of high-Vdd devices were prepared by using a triple-gate-oxide process. Moreover, for mixed signal application, Ta_2O_5 MIM capacitors were introduced into Cu and low-k interconnects. The fourth paper was "Barrier-metal-free (BMF), Cu Dual-damascene Interconnects with Cu-epi-contacts buried in Anti-diffusive, Low-k Organic film" by NEC Corporation. BMF, Cu dual-damascene interconnects (DDI) were fabricated in plasma-polymerized, divinyl siloxane bis-benzocyclobutene (p-BCB: k=2.6) polymer film, which features anti-diffusion characteristics for the Cu. The effective dielectric constant was k_{eff}=3.1, including a very thin SiN etch-stop-layer, accomplishing 20% faster CMOS device operation than the conventional Cu-DDI in the SiO2 with Ta/TaN barriers. The last paper in the highlight session was "High-Quality Ultra-thin HfO_2 Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation" by the University of Texas. Nitridation proved useful in preventing interfacial reaction and thus improving thermal stability, as well as minimizing dopant diffusion, and improving Si surface quality. MOS capacitors and MOSFETs were fabricated on NH_3 nitrided substrates with HfO_2 dielectric and TaN gate electrode. EOT as small as 0.71 nm with the leakage current of 10^{-2} A/cm^2 at -1.5 V was obtained.

Aggressive scaling in gate length in recent years has led to research on device technologies for sub-50-nm gate length. A couple of novel technologies were proposed for such short-gate-length MOSFETs to improve performance while suppressing short-channel effects. Intel reported an asymmetric source/drain extension transistor structure. It was shown that the structure alleviated the severe drain current degradation for devices when gate-to-source/drain overlap dimensions are reduced to below 20 nm/side. Fundamental principles of device operation of asymmetric source/drain extension transistors were presented. In order to suppress short-channel effects in transistors with sub-50-nm gate length, strong halo implantation is required. However, doping concentration near source/drain regions at the surface becomes high for halo with a conventional gate structure. Therefore, mobility decreases due to impurity scattering. Fujitsu Labs presented notched-gate transistors with improved current drive and suppressed short-channel effects compared to conventional gate structures.

Integration of radio and digital functions on a single chip will enable a new generation of radio devices with potentially a very large market. To meet the targets of low cost and low power, several technologies were proposed. IBM presented a 0.13 um, partially-depleted SOI CMOS technology with optimized power-saving and RF properties. Power-saving features included low-Vt, thin-gate oxide FETs for minimum power dissipation, high-performance-at-low-voltage, high-Vt, thick-gate-oxide FETs for low-standby-power SRAM and logic-block power switches, and eight levels of Cu interconnects with low-k IDL. RF features included high f_T of 141 GHz and f_{max} of 98 GHz

High-k gate dielectrics have attracted a great deal of attention for gate dielectric application. Important issues that must be considered when incorporating high-k gate dielectrics into CMOS technology are mobility, leakage current, reliability, and process compatibility. At the symposium, there were several exciting reports on high-k dielectrics, which discussed dopant penetration, reliability with dual poly-Si gate electrodes, and thermal stability.

To fully enjoy ultrathin gate dielectrics made of high-k materials, depletion in gate electrodes should be minimized. Poly-Si gate technology becomes problematic as gate length is scaled to sub-50 nm. Metal gates are promising for suppressing depletion in the gate electrodes; however, it is necessary to achieve two gate work functions similar to those of n^+ and p^+ poly-Si. The dual-metal-gate process seems to be hard for apply practically because of its complexity and reliability issues. The University of California, Berkerley reported a single metal gate process for N/PMOSFETs. (110)-Mo was used for PMOSFETs along with nitrogen implantation, and they succeeded in reducing the Mo work function to meet the requirement of NMOSFETs. The change in the Mo work function was controlled by the nitrogen implant parameters. This is potentially useful for metal-gate CMOS transistors. Toshiba presented a buried-channel to control threshold voltage in single metal gate transistors. Since a buried channel tends to degrade short-channel effects immunity, a very shallow and steep counter channel was formed.

Papers on 0.13-0.18-um CMOS integration were presented with Cu/low-k interconnects for systems on a chip. Infineon reported up to nine levels of Copper interconnect with the industry's first true low-k dielectric (SiLK, k=2.7), which resulted in superior interconnect performance at aggressive pitches. The low-k dielectric provided up to a 30% performance advantage for a critical path of a synthesized DSP core.

Novel device structures, such as vertical structures or strained-Si structures, are attracting much interest to alleviate scaling issues, such as short-channel effects and mobility degradation. IBM fabricated novel vertical PMOSFETs that have a strained SiGe source and a Si/SiGe/Si quantum well channel. Reduced short-channel effects and floating body effects, and enhanced drive current were demonstrated. Most vertical MOSFETs involve a sophisticated process that is not compatible with standard CMOS, thus rendering co-integration of vertical and conventional planar MOSFETs difficult. ST Microelectronics presented 40-nm vertical MOSFETs fabricated using the most standard CMOS process. At the expense of four additional steps, both planar and vertical devices were co-integrated. JSAP

Fujitsu Laboratories Ltd.